Preliminary

User's Manual (SMDK S5PV210 Rev0.0)

Development Kit

for S5PV210

Dec 02, 2009

REV 0.0

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S5PV210 RISC Microprocessor
SMDK S5PV210 User's manual, Revision 0.0

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1 INTRODUCTION

1.1 SYSTEM OVERVIEW

SMDK S5PV210 (S5PV210 Development Kit) is a platform for code development of SAMSUNG's S5PV210 16/32-bit RISC microcontroller (ARM-CORTEX A8). S5PV210 is used in hand-held devices and general applications.

The S5PV210 is a 32-bit RISC cost-effective, low power, high performance microprocessor solution for mobile phones and general applications, and integrates an ARM Cortex-A8 which implements the ARM architecture V7-A with supporting numerous peripherals.

To provide optimized Hardware (H/W) performance for the 3G and 3.5G communication services, S5PV210 adopts 64-bit internal bus architecture and includes many powerful hardware accelerators for tasks such as motion video processing, display control and scaling. Integrated Multi Format Codec (MFC) supports encoding and decoding of MPEG-1/2/4, H.263, H.264 and decoding of VC1, Divx. This Hardware accelerators support realtime video conferencing and Analog TV out, HDMI for NTSC and PAL mode

The S5PV210 has an optimized interface to external memory capable of sustaining the demanding memory bandwidths required in high-end communication services. The memory system has Flash/ ROM external memory ports for parallel access and DRAM port for high bandwidth. DRAM port can be configured to support LPDDR1(=mobile DDR), DDR2 or LPDDR2.

Flash/ROM Port supports NAND Flash, NOR-Flash, OneNAND, SRAM and ROM type external memory.

To reduce total system cost and enhance overall functionality, S5PV210 includes many hardware peripherals such as TFT 24-bit true color LCD controller, Camera Interface, MIPI DSI, CSI-2, System Manager for power management, ATA I/F, 4 UART, 24-channel DMA, 4 Timers, General I/O Ports, 3 IIS, S/PDIF, 3 IIC-BUS interface, 3 HS-SPI, USB Host 2.0, USB OTG 2.0 operating at high speed (480Mbps), 4 SD Host & High Speed Multi-Media Card Interface and 4 PLLs for clock generation.

Package on Package (POP) option with MCP is available for small form factor applications.

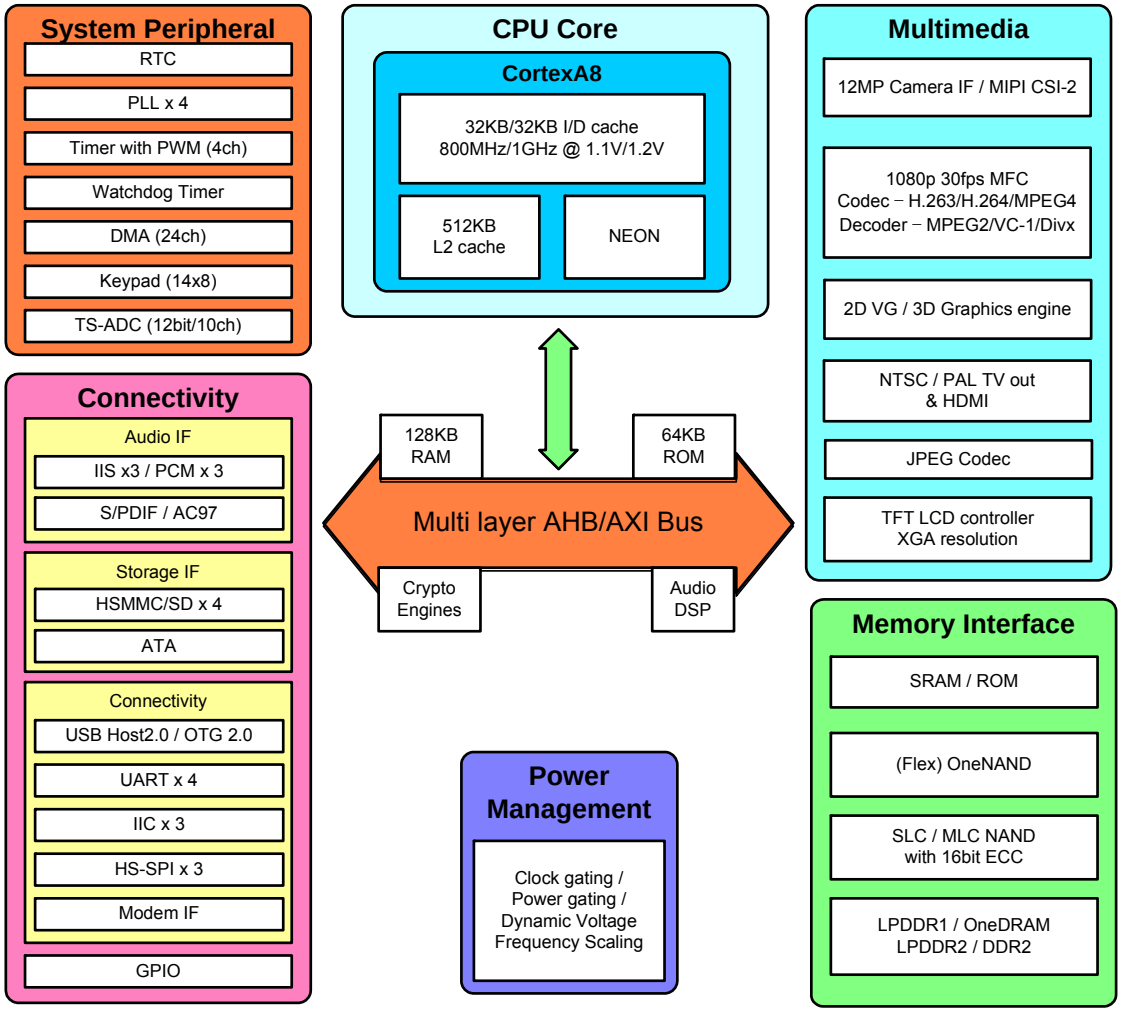


Figure 1 S5PV210 Functional Block Diagram

1.2 SMDK S5PV210 FEATURES

The SMDK S5PV210 (S5PV210 Development Kit) highlights the basic system-based hardware design which uses the S5PV210. It can evaluate the basic operations of the S5PV210 and assist in developing codes.

The features of SMDK S5PV210 include:

- Microcontroller : S5PV210 (16/32 bit RISC microcontroller, **ARM-CORTEX A8**)
- External memory
  . AMD 8Mbit NOR Flash (Socket 1EA)
  . SAMSUNG NAND Flash (Socket 1EA)
  . SAMSUNG OneNAND (External Board, Optional)
  . SAMSUNG 16Mbit SRAM 1EA
  . Dram port 0 : SAMSUNG 4 x 1Gb DDR2 SDRAM(x8)
  . Dram port 1 : SAMSUNG 4 x 1Gb DDR2 SDRAM(x8) or SAMSUNG 4 x 2Gb DDR2 SDRAM(x8)
- TFT LCD & Touch panel interface (External Board, default: 4.8" WVGA LMS480KF02)
- ATA interface (2 CF card sockets)
- SD/SDIO/MMC interface (3 SD Sockets)
- Digital Video & Audio : **HDMI 1.3 Video(720p) & S/PDIF 5.1 Channel Audio I/F**
- TV Out interface (**Composite**)
- USB Host , USB OTG 2.0 interface
- High Speed SPI interface
- IIS/AC97/PCM Interface : WM9713, WM8580 Audio CODEC on board
- General Camera Interface : 2 port
- MIPI Camera Interface : **MIPI-CSI2** (1Gbps/Lane Serial Communication)
- High Speed Serial MIPI Interface LCD : **MIPI-DSI** (1Gbps/Lane Serial Communication)
- Keypad interface
- Ethernet Interface : DM9000(10/100Mbps Ethernet controller) on board
- 2 port UART interface
- JTAG port
- Module Connector (M1 ~ M4)
  . M1 (Module1): For GPS Daughter Board (UART, SPI) : Samsung GPD14B01 (SiRFSTAR III GSD3) (Optional)
  . M2 (Module2): For Mobile TV Daughter Board (SPI, IIC) or HD Radio (SPI, IIS)
  Mobile TV: Samsung S5P4F31 (TBD, Optional)
  HD Radio: SiPORT SD1010 (TBD, Optional) , Samsung (TBD, Optional)
  . M3 (Module3): For Bluetooth Daughter Board (UART, PCM for PMIC Audio Codec)
  . M4 (Module4): For Audio Daughter Board (AC97, IIS, IIC)

2 SMDK S5PV210 REAL VIEW

2.1 SMDK S5PV210 CPU BOARD REAL VIEW

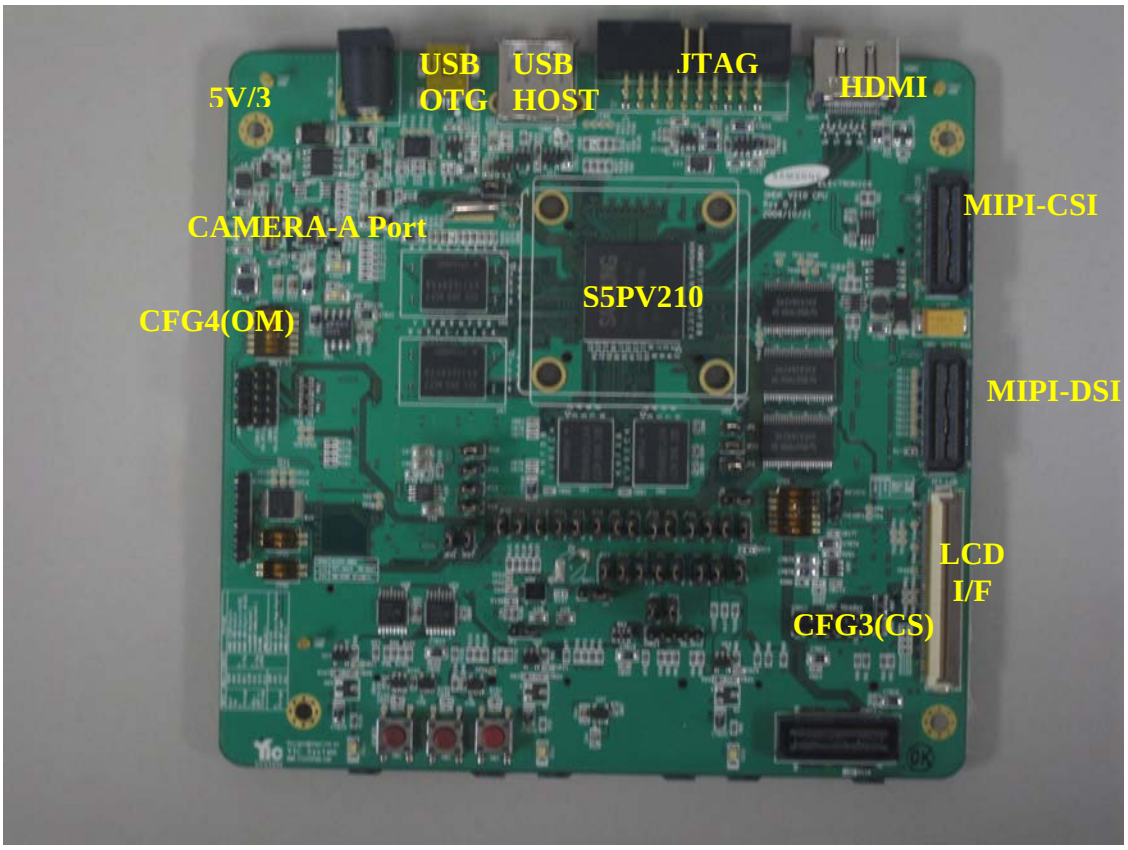


Figure 2 S5PV210 CPU BOARD TOP VIEW

External OneNAND

POWER RESET

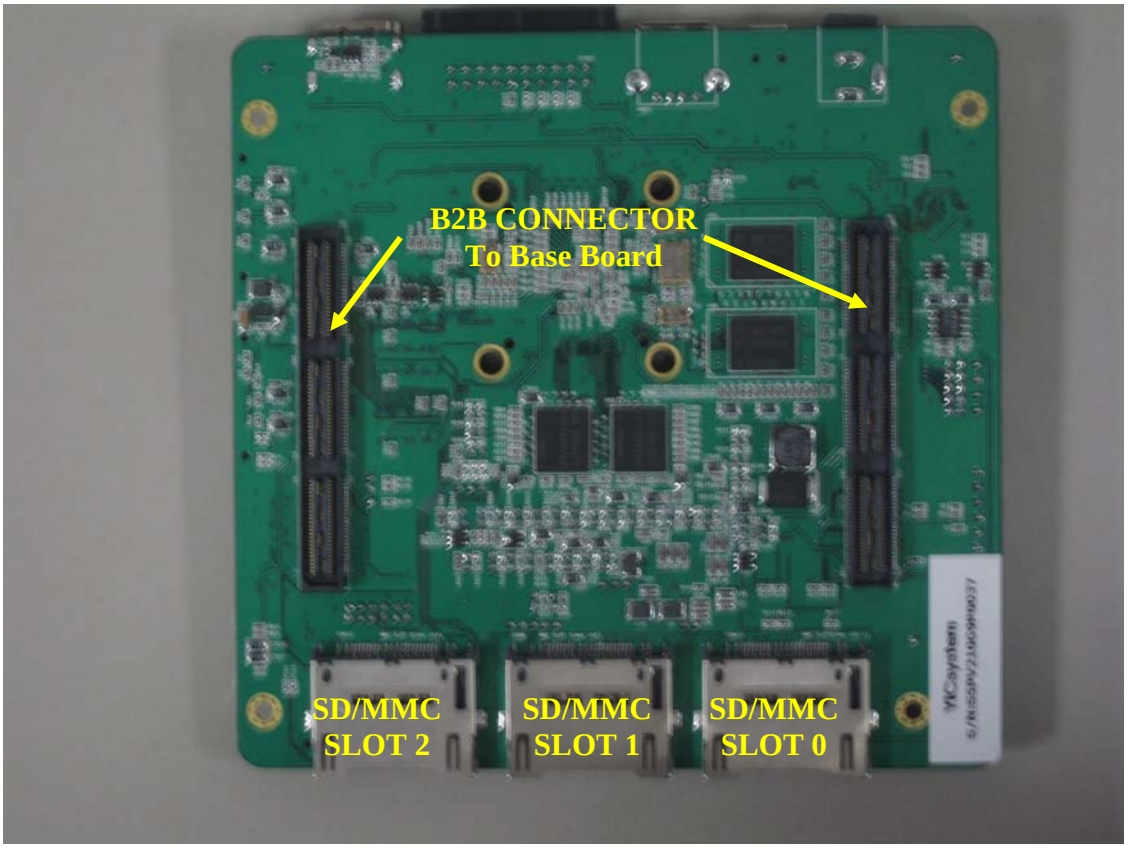


Figure 3 S5PV210 CPU BOARD BOTTOM VIEW

2.2 SMDK S5PV210 BASE BOARD REAL VIEW

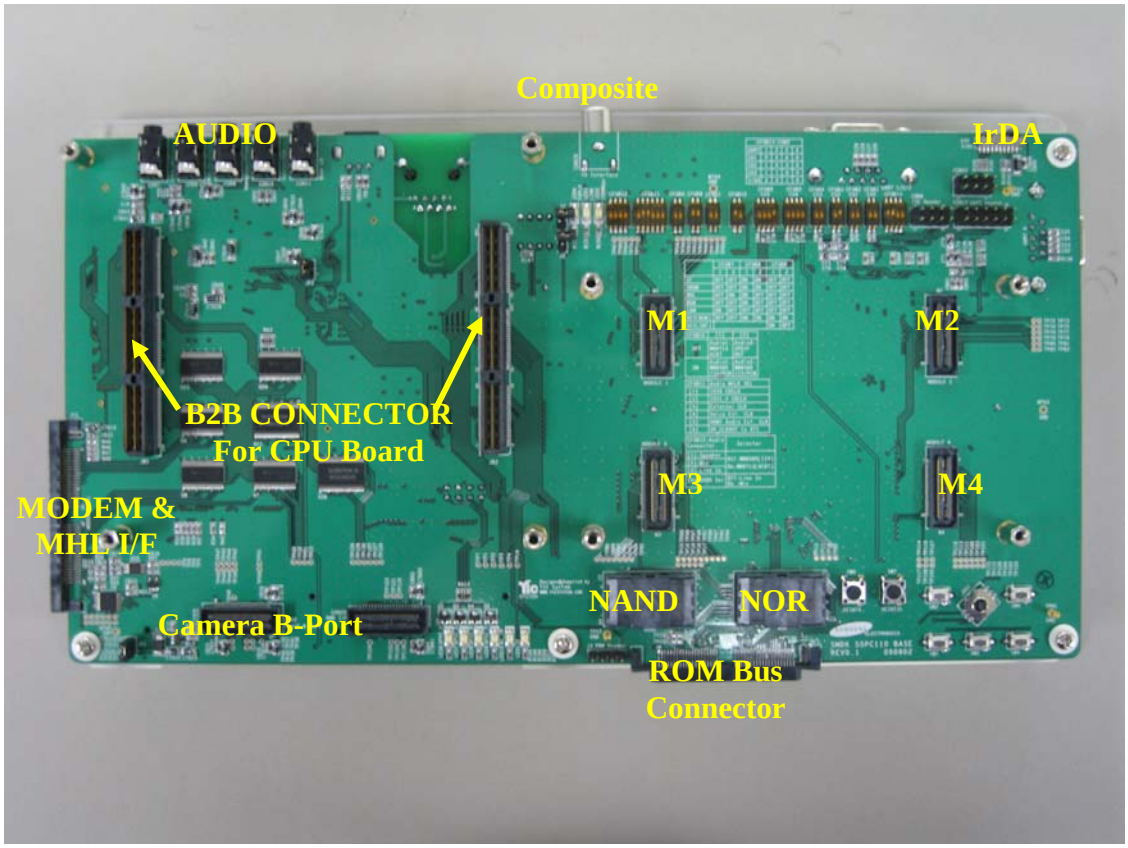


Figure 4 S5PV210 BASE BOARD TOP VIEW

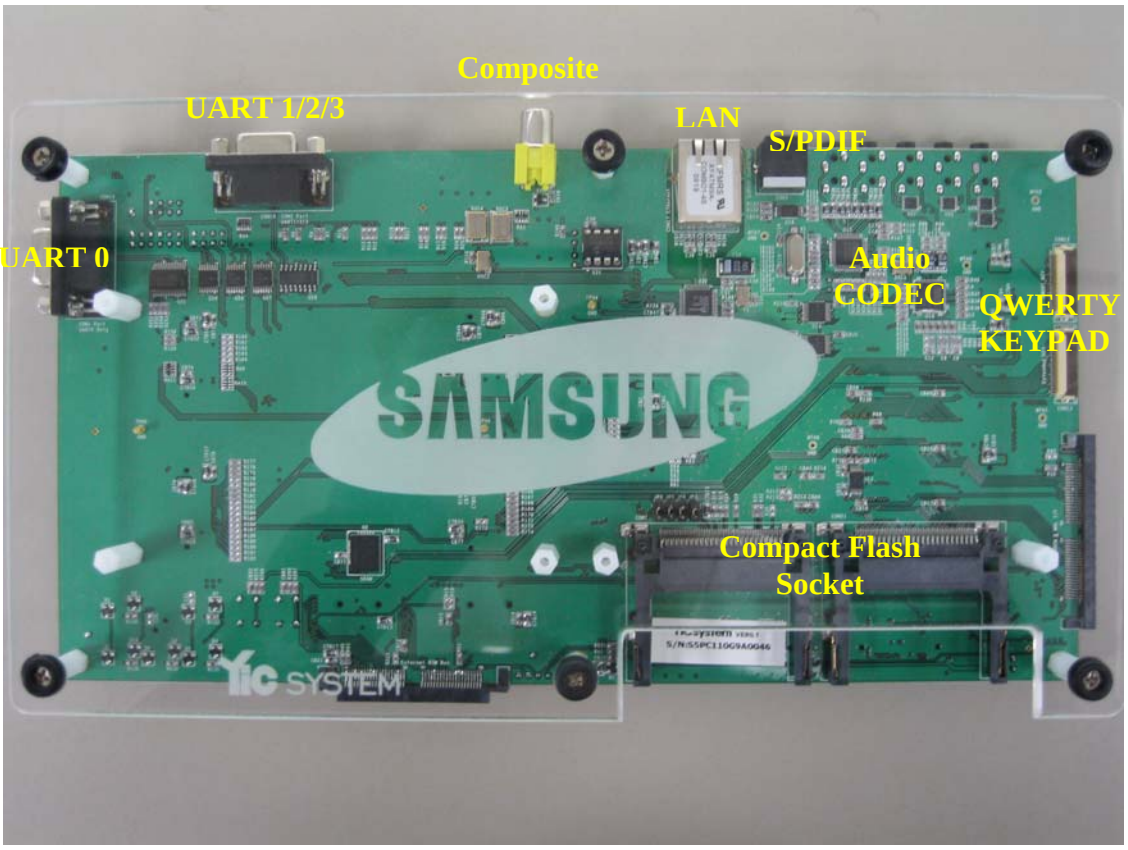


Figure 5 S5PV210 BASE BOARD BOTTOM VIEW

2.3 SMDK S5PV210 LCD BOARD REAL VIEW

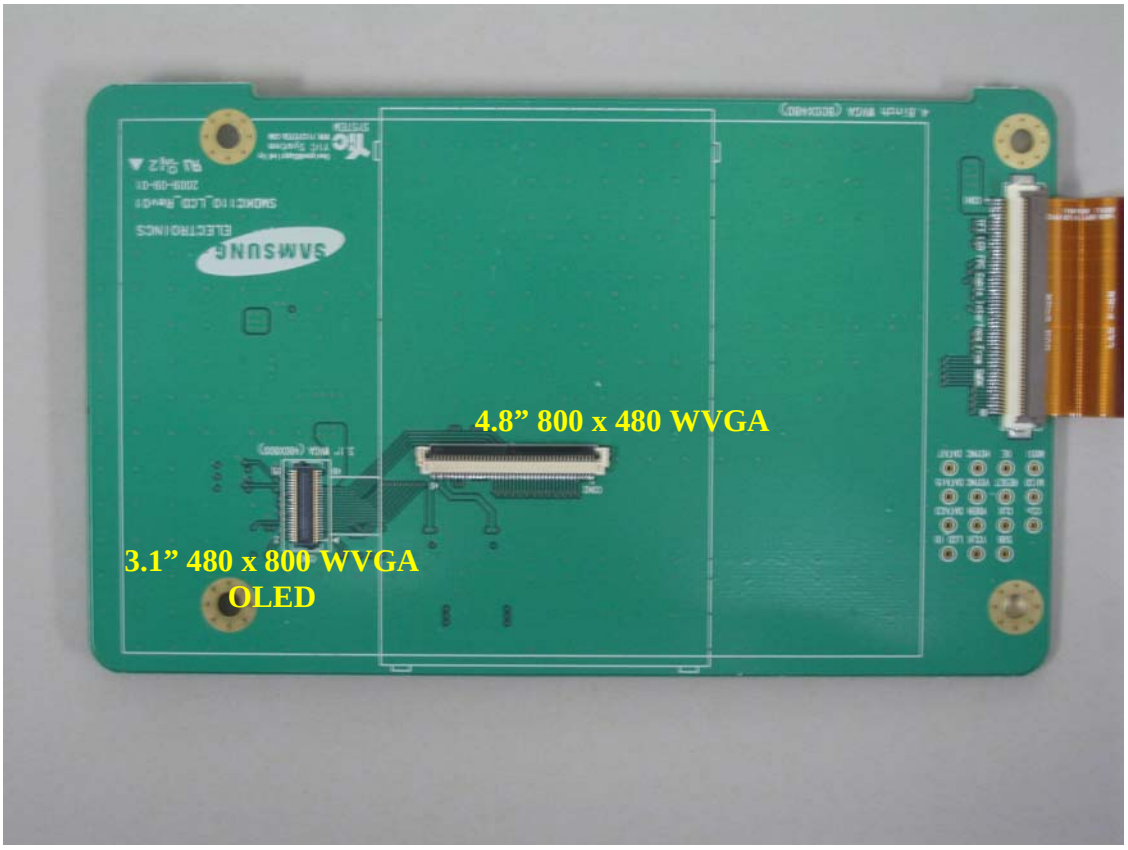


Figure 6 S5PV210 LCD BOARD TOP VIEW

3 CIRCUIT DESCRIPTION

The SMDK S5PV210 is designed to test S5PV210 and develop software while hardware is being developed. Figure 10 highlights the SMDK S5PV210's block diagram.

3.1 POWER DISTRIBUTION TREE

SMDK S5PV210 is operated by 1.1V for Internal, 1.8V for Memory and 3.3V for Input/Output pad and several peripherals. SMDK S5PV210 is supplied by 5V/3A DC Adaptor Power. The SMDK S5PV210 has distributed power plane, with power going separately to the MCU and the main power plane.

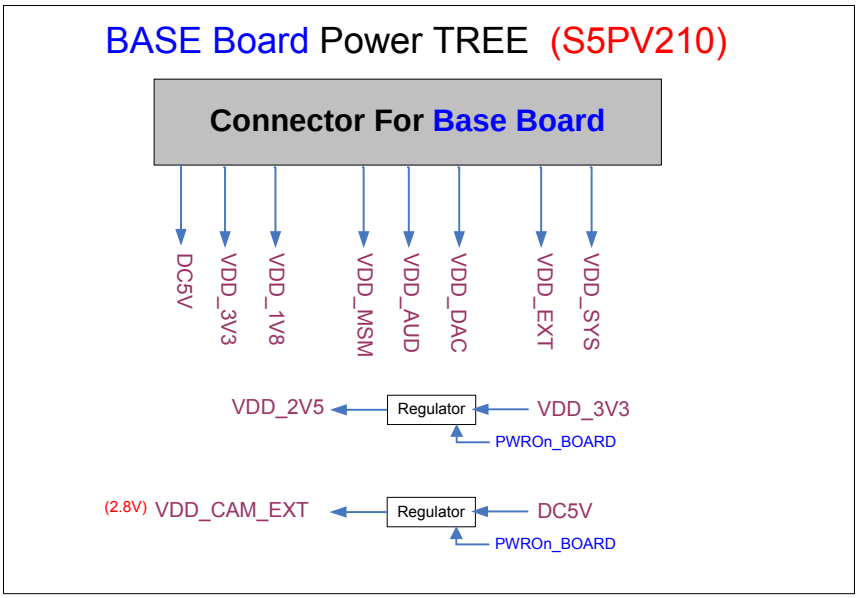


Figure 7 S5PV210 BASE BOARD POWER DISTRIBUTION TREE

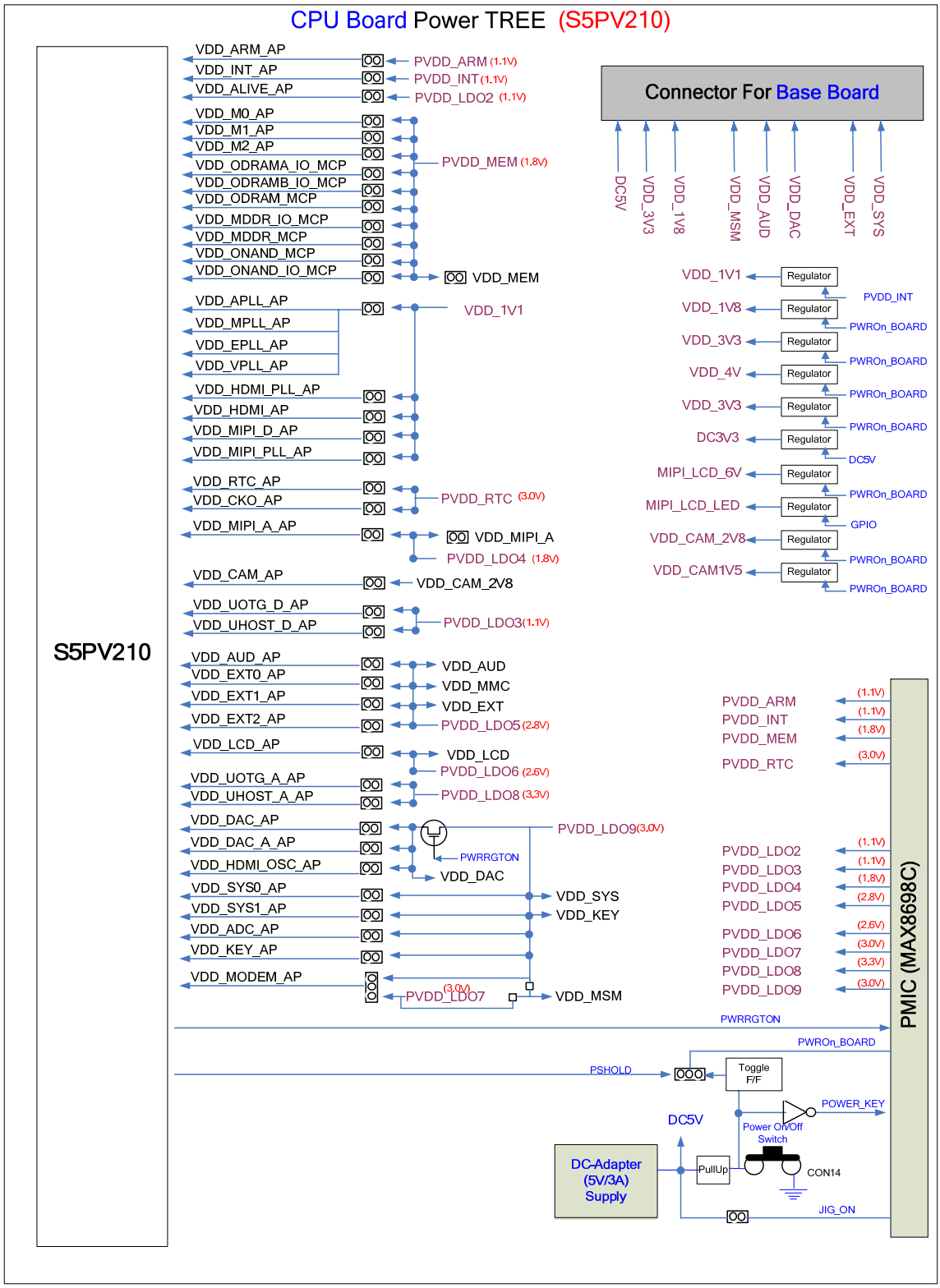


Figure 8 S5PV210 CPU BOARD POWER DISTRIBUTION TREE

3.2 FUNCTIONAL BLOCK DIAGRAM

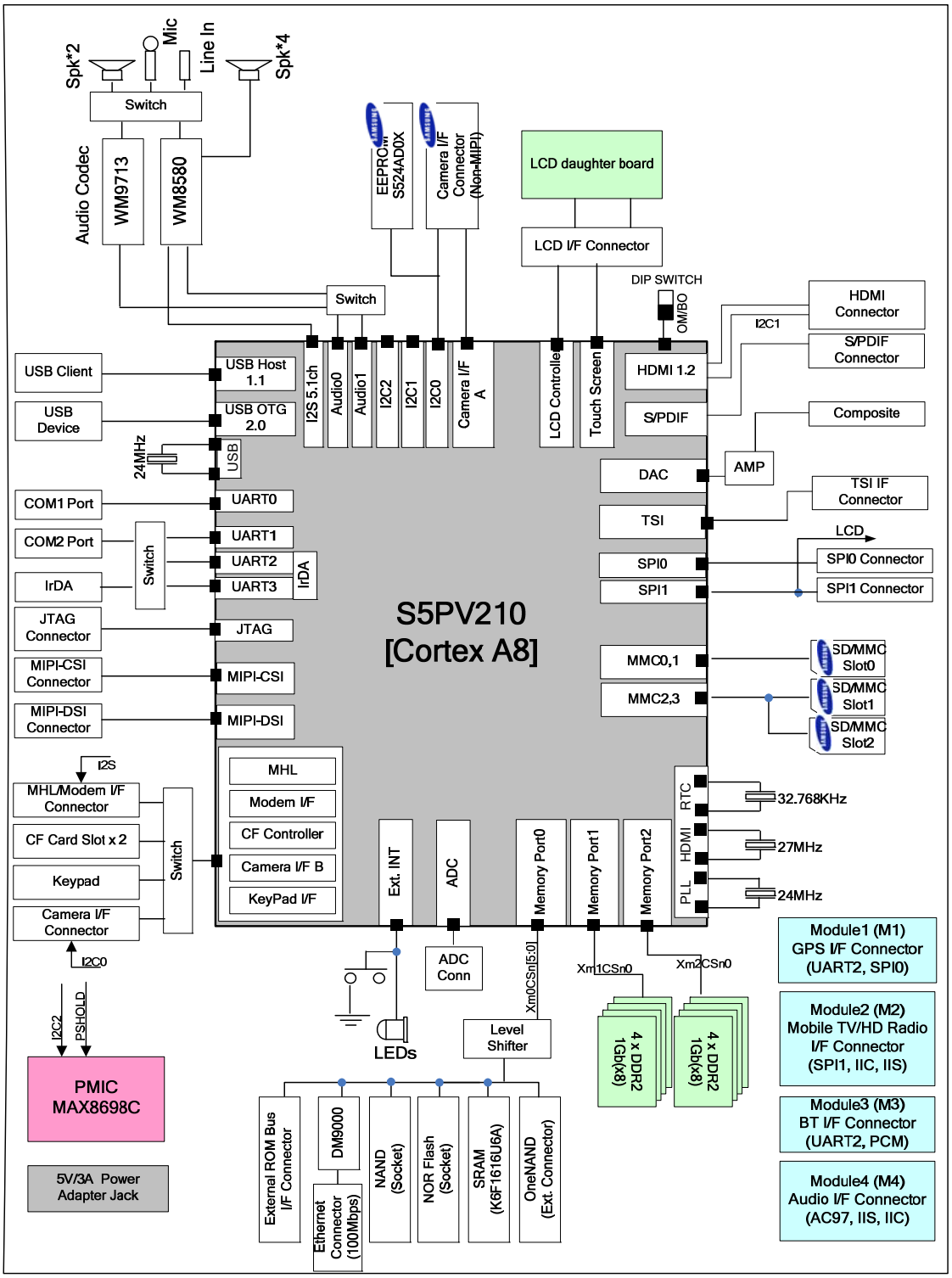


Figure 9 S5PV210 SMDK FUNCTIONAL BLOCK DIAGRAM

4 SMDK S5PV210 SYSTEM CONFIGURATIONS

Perform the following steps to use SMDK S5PV210 board.
- **CFG** is on CPU board and **CFGB** is on Base board.
- Configuration value meaning - **X**: don't care, **1**: ON **0**: OFF

Configuration Switch (DIP Switch)

Off(Switch Open) → On (Switch Short)

1. Select the Clock source(CFG4)

   Please refer to 'PLL CLOCK SOURCE SELECTION'

2. Select the Boot Device(storage) and set Boot Mode configuration switches (CFG4)

   Please refer to 'BOOT MODE SELECTION'

3. Set the CFG switch or Jumper for each booting device.

External OneNAND

- Check If OneNAND daughter card is connected on **CON14**(on CPU board).
- Set CFG3[6:1] to X0X010. (Xm0CSn4)

CFG3					
CS5			CS4		
[6]	[5]	[4]	[3]	[2]	[1]
X	OFF	X	OFF	**ON**	OFF

- Set J2(on CPU board) to 1-2 SHORT.

J2	

-

SD/MMC or eMMC

- Insert a Card to **HS-MMC slot0** (CON13 on CPU board).

- Set CFG2[2:1] to X0. (to use SDMMC channel 0 of S5PV210)

CFG2	Description
[1]	OFF

NAND Flash

- Insert a NAND Flash to **NAND socket** (U4 on Baseboard).
- Set CFGB3[2:1] to 10. (Xm0CSn2)

CFGB3	
[2]	[1]
ON	OFF

NOR Flash

- Insert a NOR Flash to **NOR socket** (U3 on Baseboard).
- Set CFGB1[2:1] to 01. (Xm0CSn0)

CFGB1	
[2]	[1]
OFF	**ON**

- Set CFGB7[2:1] to 00 and CFGB8[2:1] to 11 and CFGB9[2:1] to 00. (to use SROM Addr [16:22])

CFGB7	
[2]	[1]
OFF	OFF

CFGB8	
[2]	[1]
ON	**ON**

CFGB9	
[2]	[1]
OFF	OFF

4. Set CFGB13 for debugging message channel .

UART ch2 is for default debugging message channel and booting channel.(ch3 in case of EVT0)

- Connect to UART cable to **COM2**(CON15 on Base board)
- Set CFGB13[4:1] to 0001

CFGB13	[4]	[3]	[2]	[1]
UART2	OFF	OFF	OFF	**ON**

5. Check default Jumper setting.

<CPU Board>

- JP1~40 Short
- J4 1-2 short
- J5 1-2 short
- J8 2-3 short
- JP41 Open

<BASE Board>

- JP1 Short
- J1,J2 Open

6. Connect 5V power adapter and push the power button.
7. Check the Power LED if it is operating normally.

Refer to LED description section.

4.1 PLL CLOCK SOURCE SELECTION

Main input clock for the S5PV210 system can be selected by setting the XOM[0] values.

Description	**CFG4[1] , (XOM[0])**
24MHz X-tal Clock (XXTI)	OFF
24MHz X-tal Clock (XusbXTI)	ON (**default)**

4.2 BOOT MODE SELECTION

4.2.1 Switch Configuration

<table>
<tr><th colspan="2">Description</th><th colspan="5">CFG4[6:2]</th></tr>
<tr><td>CFG4[6]</td><td>CFG4[5:2]</td><td>CFG4[6]</td><td>CFG4[5]</td><td>CFG4[4]</td><td>CFG4[3]</td><td>CFG4[2]</td></tr>
<tr><td rowspan="14">I-ROM Booting sequence: Storage</td><td>eSSD</td><td rowspan="14">OFF</td><td rowspan="8">OFF</td><td rowspan="6">OFF</td><td rowspan="2">OFF</td><td>OFF</td></tr>
<tr><td>Nand 2KB, 5cycle
(Nand 8bit ECC)</td><td>ON</td></tr>
<tr><td>Nand 4KB, 5cycle
(Nand 8bit ECC)</td><td rowspan="2">ON</td><td>OFF</td></tr>
<tr><td>Nand 4KB, 5cycle
(Nand 16bit ECC)</td><td>ON</td></tr>
<tr><td>OnenandMux</td><td rowspan="4">ON</td><td rowspan="2">OFF</td><td>OFF</td></tr>
<tr><td>OnenandDemux</td><td>ON</td></tr>
<tr><td>SD/MMC</td><td rowspan="2">ON</td><td>OFF</td></tr>
<tr><td>eMMC(4-bit)</td><td>ON</td></tr>
<tr><td>Reserved</td><td rowspan="4">ON</td><td rowspan="4">OFF</td><td rowspan="2">OFF</td><td>ON</td></tr>
<tr><td>Nand 2KB, 4cycle
(Nand 8bit ECC)</td><td>ON</td></tr>
<tr><td>NOR boot</td><td rowspan="2">ON</td><td>OFF</td></tr>
<tr><td>eMMC(8-bit)</td><td>ON</td></tr>
<tr><td rowspan="2">I-ROM Booting sequence:</td><td>eSSD</td><td>ON</td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td></tr>
<tr><td>Nand 2KB, 5cycle</td><td colspan="4">ON</td></tr>
</table>

UART ->USB ->Storage						
	Nand 4KB, 5cycle				**ON**	OFF
	Nand 4KB, 5cycle (Nand 16bit ECC)					**ON**
	OnenandMux(Audi)			**ON**	OFF	OFF
	OnenandDemux(Audi)					**ON**
	SD/MMC				**ON**	OFF
	eMMC(4-bit)					**ON**

Note) If CFG4[6] is set to 1, It is used for debug mode that UART boot is first and USB boot is second. UART boot has some kind of error case. In case of UART error, the iROM boot sequence moves to USB boot. USB boot also has some kind of error case like UART. If USB boot is fail, boot sequence move to main storage boot.
Please refer to iROM application note which is more detail about error case.

4.3 CONFIGURATION SWITCH DESCRIPTION IN CPU BOARD

4.3.1 CFG3: SELECTION FOR CS#4,#5

	CFG3					
Description	**CS5**			**CS4**		
	[6]	[5]	[4]	[3]	[2]	[1]
ON		*External OneNand*	**Connect to Base CS#5**		External OneNand	Connect to Base CS#4

4.3.2 J2: SELECTION for Interrupt of Ext. OneNAND

J2	***Description***
1-2 short	Connect to ONDXL_INT0
2-3 short	Connect to ONDXL_INT1(**default)**

4.3.3 CFG2: Configuration of MMC slot 0

CFG2	*Description*
[1]	ON : MMC port 1 4bit Data Width OFF : MMC port 0 8bit Data Width (**default)**
[2]	ON : HDMI I2C Buffer Disable OFF : HDMI I2C Buffer Enable

4.3.4 CFG1: TSI I/F

CFG3	*Description*
[1]	ON : TSI I/F Buffer Enable OFF : TSI I/F Buffer Disable
[2]	ON : TSI RX OFF : TSI TX

4.3.5 J3: PSHOLD selection

J3	*Description*
1-2 short	Not using PSHOLD
2-3 short	Using PSHOLD. PSHOLD should be programmed Output-HIGH during pressing the power button ,.

4.3.6 JP1: JIG ON selection

JIG ON is used to turn on board without pressing power button.

JP1	*Description*
short	Turn on system power always.
open	Turn on system power by pressing power button.

4.4 CONFIGURATION SWITCH DESCRIPTION IN BASE BOARD

4.4.1 CFGB1: SROM BANK0 CHIP SELECTOR

CFGB1 component is used to select devices as SROM BUS I/F 0(B_Xm0CSn0).

Description	**CFGB1**	
	[2]	[1]
NOR (AMD) Flash	OFF	**ON**
SRAM	**ON**	OFF

4.4.2 CFGB2: SROM BANK1 CHIP SELECTOR

CFGB2 component is used to select devices as SROM BUS I/F 1(B_Xm0CSn1).

Description	**CFGB2**	
	[2]	[1]
NOR (AMD) Flash	OFF	**ON**
SRAM	**ON**	OFF

4.4.3 CFGB3: SROM BANK2 CHIP SELECTOR

CFGB3 component is used to select devices as SROM BUS I/F 2(B_Xm0CSn2/NFCSn0).

Description	**CFGB3**	
	[2]	[1]
SRAM	OFF	**ON**
Nand CS 0	**ON**	OFF

4.4.4 CFGB4: SROM BANK3 CHIP SELECTOR

CFGB4 component is used to select devices as SROM BUS I/F 3(B_Xm0CSn3/NFCSn1).

Description	**CFGB4**	
	[2]	[1]
SRAM	OFF	**ON**

Nand CS 1	**ON**	OFF

4.4.5 CFGB5: SROM BANK4 CHIP SELECTOR

CFGB5 component is used to select devices as SROM BUS I/F 4(B_Xm0CSn4/NFCSn2).

Description	**CFGB5**			
	[4]	[3]	[2]	[1]
SRAM	OFF	OFF	OFF	**ON**
NAND CS 2	OFF	OFF	**ON**	OFF
External Rom Bus Connector	OFF	**ON**	OFF	OFF
Ethernet	**ON**	OFF	OFF	OFF

4.4.6 CFGB6: SROM BANK5 CHIP SELECTOR

CFGB6 component is used to select devices as SROM BUS I/F 5(B_Xm0CSn5/NFCSn3).

Description	**CFGB6**			
	[4]	[3]	[2]	[1]
SRAM	OFF	OFF	OFF	**ON**
NAND CS 3	OFF	OFF	**ON**	OFF
External Rom Bus Connector	OFF	**ON**	OFF	OFF
Ethernet	**ON**	OFF	OFF	OFF

4.4.7 CF,MODEM,CAM_B,KEY,MHL,SROM ADDR SWITCHING

CFGB7,8,9 component is used to switching Xmsm signals which are muxed following signals.

(CF Card I/F, Modem I/F, Camera B I/F, Keypad I/F, MHL I/F, SROM Addr[16:22])

Description	**CFGB7**	**CFGB8**	**CFGB9**

	[1]	[2]	[1]	[2]	[1]	[2]
CF Card	OFF	OFF	**ON**	**ON**	ON/OFF	OFF
SROM Addr [22:16]	OFF	OFF	**ON**	**ON**	ON/OFF	OFF
MHL I/F	OFF	**ON**	**ON**	OFF	ON/OFF	OFF
MODEM I/F	OFF	OFF	**ON**	OFF	ON/OFF	OFF
Camera B port	**ON**	OFF	OFF	OFF	ON/OFF	OFF
Keypad muxed with Xmsm signals	OFF	OFF	**ON**	**ON**	**ON**	**ON**
Keypad muxed with XEINT signals					**ON**	OFF

4.4.8 CFGB10: Audio Port

CFGB10 component is used to select devices as Audio I/F 1,2.

Description	**Audio2**	**Audio1**
	[2]	[1]
OFF	SPDIF Out	**AC97(WM9713)**
ON	**IIS/PCM(WM8580)**	IIS/PCM(WM8580)

4.4.9 CFGB11: Audio Codec(WM8580) Master clock selection

CFGB11	***Mater Clock source***
[1]	I2S0 CDCLK
[2]	I2S1,2 CDCLK
[3]	External CLK
[4]	External Voice CLK
[5]	External HDMI Audio CLK
[6]	AP CLKOUT

4.4.10 CFGB12: Audio Device Input/Output Connection

CFGB12	*Description*
[1] : Speaker	OFF: IIS (WM8580) ON: AC97 (WM9713)
[2] : MIC	
[3] : Line In	
[4] : WM8580	OFF: Line In ON: MIC

4.4.11 CFGB13: UART/IrDA Connection

CFGB13 component is used to select COM2(CON15) Port connection.

CFGB13	[1]	[2]	[3]	[4]
UART1	OFF	X	X	X
UART2	ON	OFF	X	X
UART3	ON	ON	OFF	X
IrDA	X	X	ON	X

4.5 LED & SWITCH Description

4.5.1 LED description

<CPU Board>

1. LED4: 5V Power(adapter) Status
2. LED5: System power(from PMIC) Status

3. LED3: Card Insertion status of MMC slot 0
4. LED1: Card Insertion status of MMC slot 1
5. LED2: Card Insertion status of MMC slot 2

<Base Board>

6. LED1: CF card Power status
7. LED2,3,4: Ethernet status
8. LED6: For debugging (GPH2_4)
9. LED7: For debugging (GPH2_5)
10. LED8: For debugging (GPH2_6)
11. LED9: For debugging (GPH2_7)
12. LED10: 5V Power(adapter) Status

4.5.2 Switch description

<CPU Board>

1. SW2 : Warm reset switch
2. SW3: System reset switch
3. SW1: Power On switch

<Base Board>

4. SW6 : For EINT test (XEINT4)
5. SW7 : For EINT test (XEINT31)

5 SMDK Daughter Board

Each Daughter board can be connected on SMDK connector.

5.1 External OneNAND

External OneNAND can be mounted on **CON14**.

5.1.1 Real view

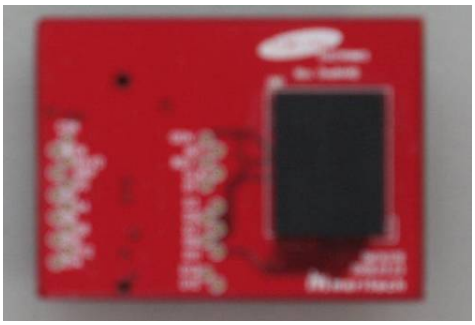


Figure 10 External OneNAND

5.1.2 Schematic

EXTERNAL_ONENAND.pdf

5.2 CSI Daughter Board

CSI Daughter Board can be mounted on **CON2**.

5.2.1 Real view

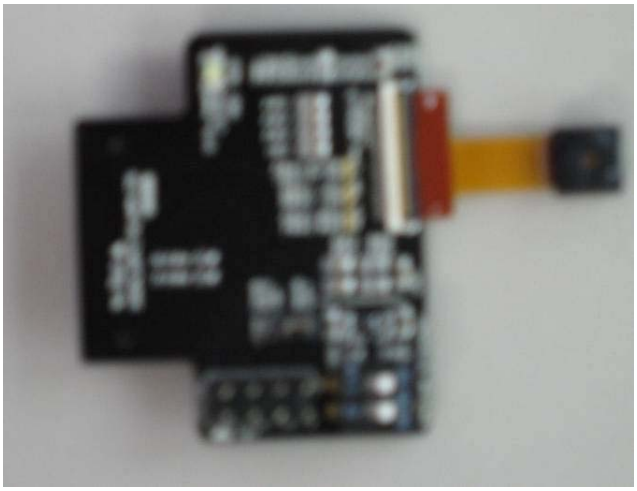


Figure 11 CSI Daughter Board

5.2.2 Schematic

CSI_daughter_BOARD.pdf

5.3 DSI Daughter Board

DSI Daughter Board can be mounted on **CON1**.

5.3.1 Real view

Figure 12 DSI Daughter Board

5.3.2 Schematic

MIPI-LCM&LAN_
BD_SCHEMATIC_I

6 SMDK SCHEMATIC REVISION HISTORY

This document contains information of corrected points on the schematic of SMDK S5PV210.

Boards	Page	Contents	Corrected points (ECN)
CPU Board			
Base Board			
LCD Board			

7 SMDK SCHEMATIC

There are 3 parts of SMDK Schematic.

1. CPU & Base Board Rev0.1
2. LCD Board Rev0.1


SMDKV210_CPU_REV0_1.pdf


SMDKV210_BASE_BD_SCH_REV01.p


S5PV210_SMDK_LCD_SCHEMATIC_

SMDK_S5PV210_CPU B'd (S5PV210 Evaluation Board) Schematics

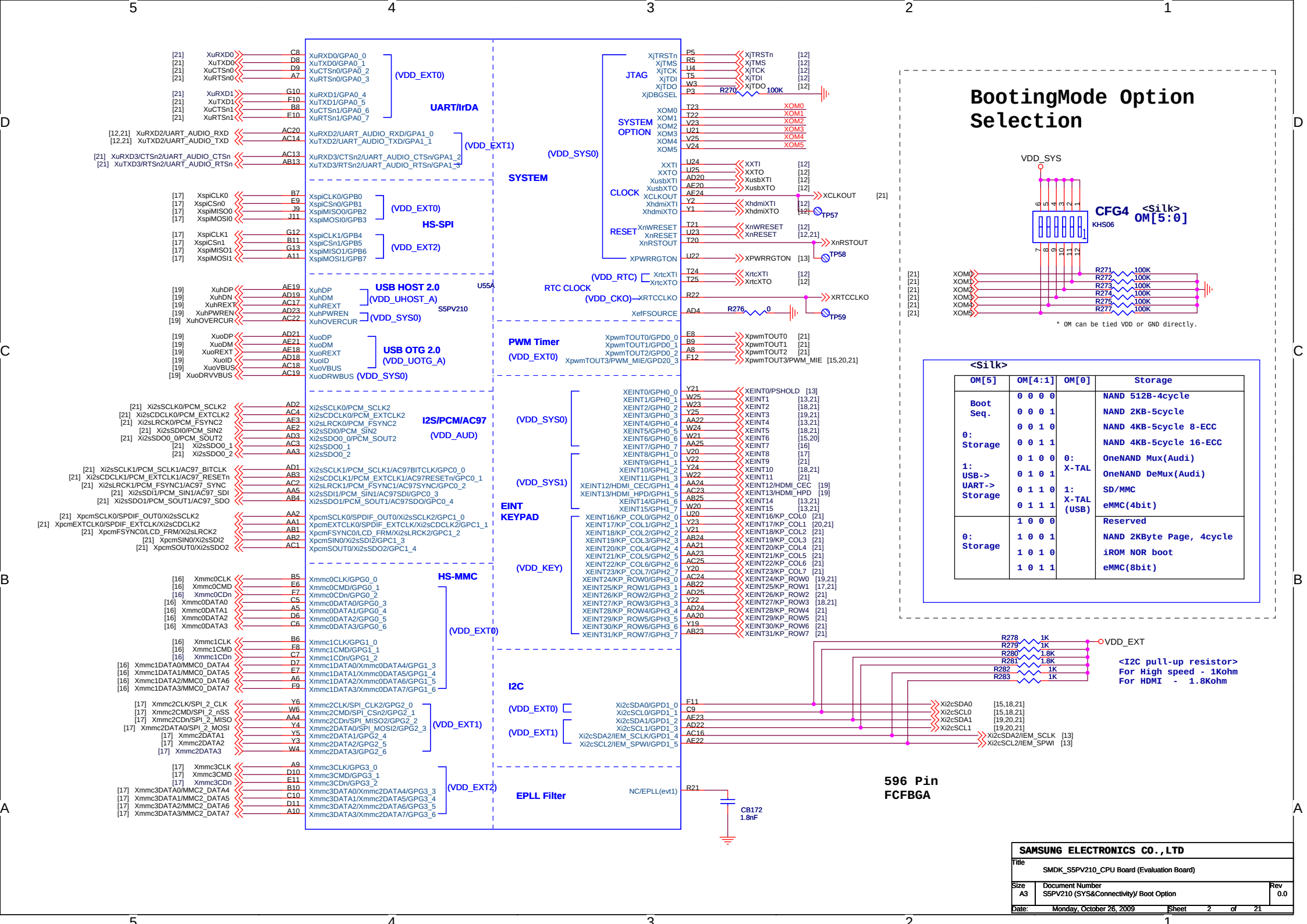
Revision	Date	Description
Rev 0.0	2009. 09	Preliminary Version

Table of Contents

Part Reference

<Component><Number>
U : Component or Regurator IC
C : Capacitor
CB : Capacitor Bypass
CT : Capacitor Tantal
CTB : Capacitor Tantal Bypass
J : Jumper
JB : CPU To Base connector
JP : Jumper Power
R : Resistor
RA : Resistor Array
RP : Resistor Power
VR : Variable Resistor
L : Inductor
FB : Ferrite Bead
OSC : Oscillator
X : X-tal (Crystal)
Q : Transistor or FET
D : Diode
ZD : Zener Diode
LED : LED Diode
SW : SWitch Tact/Push
CON : CONnector
CFG : ConFiGure switch (DIP/Slide)
TP : Test Point (SMD)
TPH : Test Point Hole (Through Hole)
MTH: Mount Through Hole
MOD : MODule Interface connector

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PV210_CPU Board (Evaluation Board)		
Size: A3	Document Number: Revision History	Rev: 0.0
Date: Monday, October 26, 2009	Sheet 1 of 21	


UART/IrDA
(VDD_EXT0)
(VDD_EXT1)
HS-SPI
(VDD_EXT0)
(VDD_EXT2)
USB HOST 2.0
(VDD_UHOST_A)
(VDD_SYS0)
S5PV210
USB OTG 2.0
(VDD_UOTG_A)
(VDD_SYS0)
I2S/PCM/AC97
(VDD_AUD)
HS-MMC
(VDD_EXT0)
(VDD_EXT1)
(VDD_EXT2)
SYSTEM
(VDD_SYS0)
JTAG
SYSTEM OPTION
CLOCK
RESET
(VDD_RTC)
RTC CLOCK
(VDD_CKO)
PWM Timer
(VDD_EXT0)
EINT
KEYPAD
(VDD_SYS0)
(VDD_SYS1)
(VDD_KEY)
I2C
(VDD_EXT0)
(VDD_EXT1)
EPLL Filter
BootingMode Option Selection
VDD_SYS
CFG4
KHS06
<Silk>
OM[5:0]
* OM can be tied VDD or GND directly.
<Silk>
OM[5] OM[4:1] OM[0] Storage
Boot Seq. 0: Storage 0 0 0 0 NAND 512B-4cycle
0 0 0 1 NAND 2KB-5cycle
0 0 1 0 NAND 4KB-5cycle 8-ECC
0 0 1 1 NAND 4KB-5cycle 16-ECC
1: USB-> UART-> Storage 0 1 0 0 0: X-TAL OneNAND Mux(Audi)
0 1 0 1 OneNAND DeMux(Audi)
0 1 1 0 1: X-TAL (USB) SD/MMC
0 1 1 1 eMMC(4bit)
0: Storage 1 0 0 0 Reserved
1 0 0 1 NAND 2KByte Page, 4cycle
1 0 1 0 iROM NOR boot
1 0 1 1 eMMC(8bit)
<I2C pull-up resistor>
For High speed - 1Kohm
For HDMI - 1.8Kohm
596 Pin
FCFBGA
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK_S5PV210_CPU Board (Evaluation Board)
Size A3
Document Number
S5PV210 (SYS&Connectivity)/ Boot Option
Rev 0.0
Date: Monday, October 26, 2009
Sheet 2 of 21

XM1,2 MEMORY Interface
OneNAND Interface

Memory Port0
SROM/NAND/ONENAND
(VDD_M0)

U55B
S5PV210

Memory Port1
DDR2/mDDR/mDDR2
(VDD_M1)

Memory Port2
DDR2/mDDR/mDDR2
(VDD_M2)

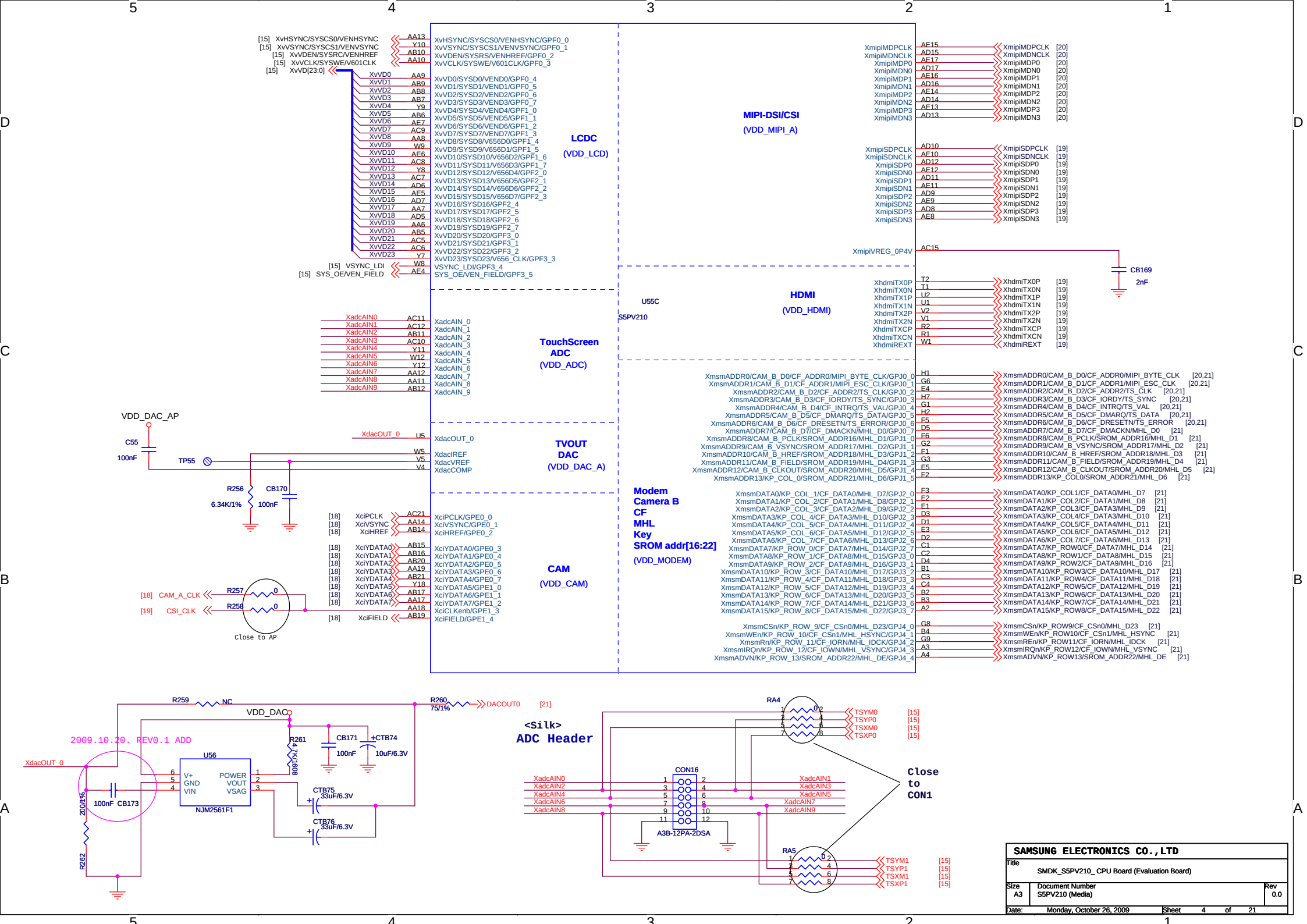
XDDR2SEL
(VDD_SYS0)

VDD_MEM
VDD_SYS

R263 4.7K
R264 4.7K
R265 4.7K
R266 4.7K
R267 4.7K
R268 100K
R269 NC

TP56

SAMSUNG ELECTRONICS CO.,LTD	
Title	SMDK_S5PV210_CPU Board (Evaluation Board)
Size: A3	Document Number: S5PV210 (DRR2 & SROM Memory) — Rev: 0.0
Date: Monday, October 26, 2009	Sheet 3 of 21


LCDC
(VDD_LCD)
MIPI-DSI/CSI
(VDD_MIPI_A)
HDMI
(VDD_HDMI)
U55C
S5PV210
TouchScreen
ADC
(VDD_ADC)
TVOUT
DAC
(VDD_DAC_A)
CAM
(VDD_CAM)
Modem
Camera B
CF
MHL
Key
SROM addr[16:22]
(VDD_MODEM)
VDD_DAC_AP
VDD_DAC
2009.10.20. REV0.1 ADD
Close to AP
<Silk>
ADC Header
CON16
A3B-12PA-2DSA
Close
to
CON1
NJM2561F1
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK_S5PV210_ CPU Board (Evaluation Board)
Size
A3
Document Number
S5PV210 (Media)
Rev
0.0
Date:
Monday, October 26, 2009
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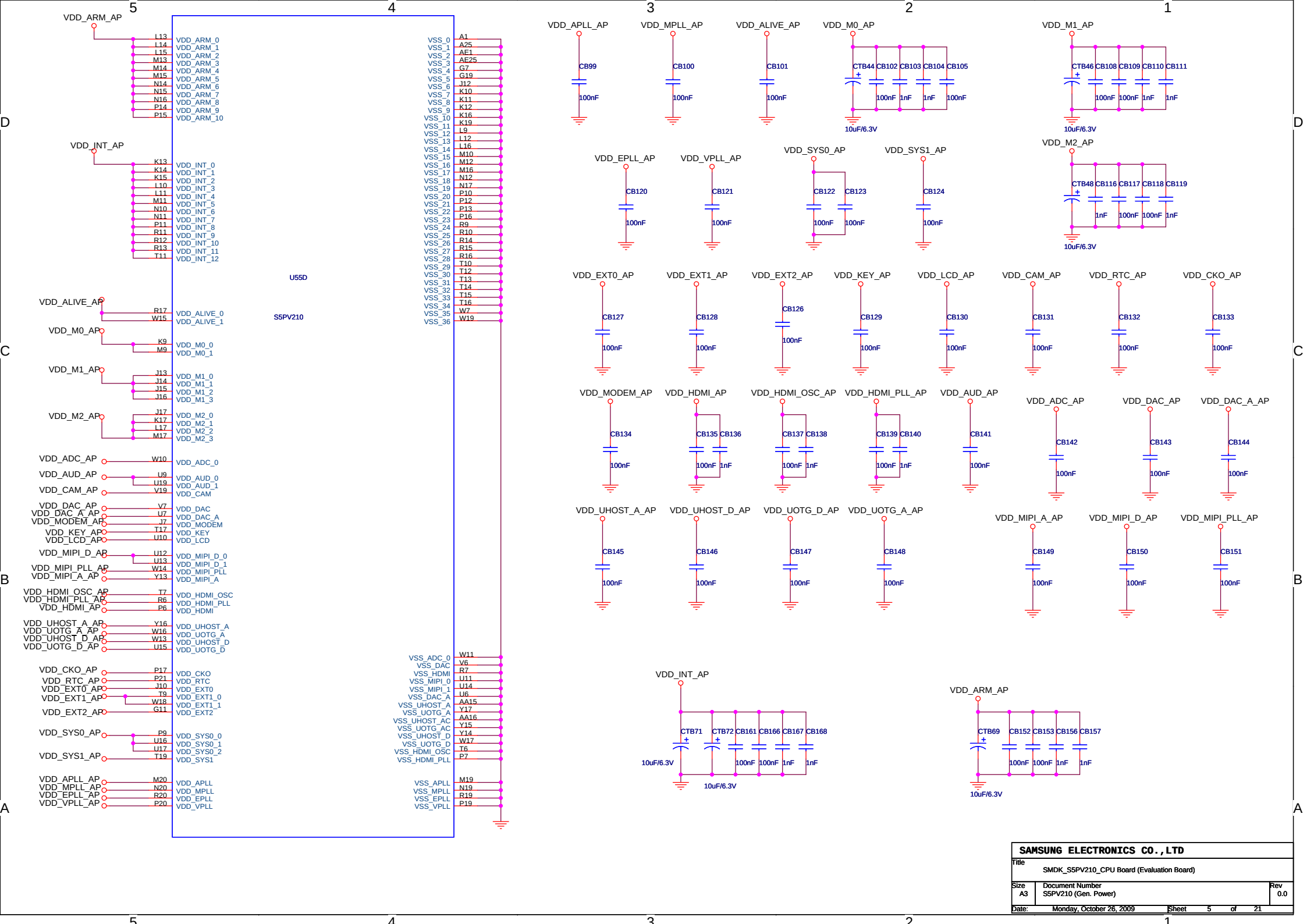
U55D
S5PV210
VDD_ARM_AP
VDD_ARM_0
VDD_ARM_1
VDD_ARM_2
VDD_ARM_3
VDD_ARM_4
VDD_ARM_5
VDD_ARM_6
VDD_ARM_7
VDD_ARM_8
VDD_ARM_9
VDD_ARM_10
VDD_INT_AP
VDD_INT_0
VDD_INT_1
VDD_INT_2
VDD_INT_3
VDD_INT_4
VDD_INT_5
VDD_INT_6
VDD_INT_7
VDD_INT_8
VDD_INT_9
VDD_INT_10
VDD_INT_11
VDD_INT_12
VDD_ALIVE_AP
VDD_ALIVE_0
VDD_ALIVE_1
VDD_M0_AP
VDD_M0_0
VDD_M0_1
VDD_M1_AP
VDD_M1_0
VDD_M1_1
VDD_M1_2
VDD_M1_3
VDD_M2_AP
VDD_M2_0
VDD_M2_1
VDD_M2_2
VDD_M2_3
VDD_ADC_AP
VDD_ADC_0
VDD_AUD_AP
VDD_AUD_0
VDD_AUD_1
VDD_CAM_AP
VDD_CAM
VDD_DAC_AP
VDD_DAC
VDD_DAC_A_AP
VDD_DAC_A
VDD_MODEM_AP
VDD_MODEM
VDD_KEY_AP
VDD_KEY
VDD_LCD_AP
VDD_LCD
VDD_MIPI_D_AP
VDD_MIPI_D_0
VDD_MIPI_D_1
VDD_MIPI_PLL_AP
VDD_MIPI_PLL
VDD_MIPI_A_AP
VDD_MIPI_A
VDD_HDMI_OSC_AP
VDD_HDMI_OSC
VDD_HDMI_PLL_AP
VDD_HDMI_PLL
VDD_HDMI_AP
VDD_HDMI
VDD_UHOST_A_AP
VDD_UHOST_A
VDD_UOTG_A_AP
VDD_UOTG_A
VDD_UHOST_D_AP
VDD_UHOST_D
VDD_UOTG_D_AP
VDD_UOTG_D
VDD_CKO_AP
VDD_CKO
VDD_RTC_AP
VDD_RTC
VDD_EXT0_AP
VDD_EXT0
VDD_EXT1_AP
VDD_EXT1_0
VDD_EXT1_1
VDD_EXT2_AP
VDD_EXT2
VDD_SYS0_AP
VDD_SYS0_0
VDD_SYS0_1
VDD_SYS0_2
VDD_SYS1_AP
VDD_SYS1
VDD_APLL_AP
VDD_MPLL_AP
VDD_EPLL_AP
VDD_VPLL_AP
VDD_APLL
VDD_MPLL
VDD_EPLL
VDD_VPLL
VSS_0
VSS_1
VSS_2
VSS_3
VSS_4
VSS_5
VSS_6
VSS_7
VSS_8
VSS_9
VSS_10
VSS_11
VSS_12
VSS_13
VSS_14
VSS_15
VSS_16
VSS_17
VSS_18
VSS_19
VSS_20
VSS_21
VSS_22
VSS_23
VSS_24
VSS_25
VSS_26
VSS_27
VSS_28
VSS_29
VSS_30
VSS_31
VSS_32
VSS_33
VSS_34
VSS_35
VSS_36
VSS_ADC_0
VSS_DAC
VSS_HDMI
VSS_MIPI_0
VSS_MIPI_1
VSS_DAC_A
VSS_UHOST_A
VSS_UOTG_A
VSS_UHOST_AC
VSS_UOTG_AC
VSS_UHOST_D
VSS_UOTG_D
VSS_HDMI_OSC
VSS_HDMI_PLL
VSS_APLL
VSS_MPLL
VSS_EPLL
VSS_VPLL
VDD_APLL_AP
VDD_MPLL_AP
VDD_ALIVE_AP
VDD_M0_AP
VDD_EPLL_AP
VDD_VPLL_AP
VDD_SYS0_AP
VDD_SYS1_AP
VDD_M1_AP
VDD_M2_AP
VDD_EXT0_AP
VDD_EXT1_AP
VDD_EXT2_AP
VDD_KEY_AP
VDD_LCD_AP
VDD_CAM_AP
VDD_RTC_AP
VDD_CKO_AP
VDD_MODEM_AP
VDD_HDMI_AP
VDD_HDMI_OSC_AP
VDD_HDMI_PLL_AP
VDD_AUD_AP
VDD_ADC_AP
VDD_DAC_AP
VDD_DAC_A_AP
VDD_UHOST_A_AP
VDD_UHOST_D_AP
VDD_UOTG_D_AP
VDD_UOTG_A_AP
VDD_MIPI_A_AP
VDD_MIPI_D_AP
VDD_MIPI_PLL_AP
VDD_INT_AP
VDD_ARM_AP
CB99
CB100
CB101
CTB44
CB102
CB103
CB104
CB105
CTB46
CB108
CB109
CB110
CB111
CB120
CB121
CB122
CB123
CB124
CTB48
CB116
CB117
CB118
CB119
CB127
CB128
CB126
CB129
CB130
CB131
CB132
CB133
CB134
CB135
CB136
CB137
CB138
CB139
CB140
CB141
CB142
CB143
CB144
CB145
CB146
CB147
CB148
CB149
CB150
CB151
CTB71
CB161
CB166
CB167
CB168
CTB69
CB152
CB153
CB156
CB157
100nF
1nF
10uF/6.3V
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK_S5PV210_CPU Board (Evaluation Board)
Size
A3
Document Number
S5PV210 (Gen. Power)
Rev
0.0
Date:
Monday, October 26, 2009
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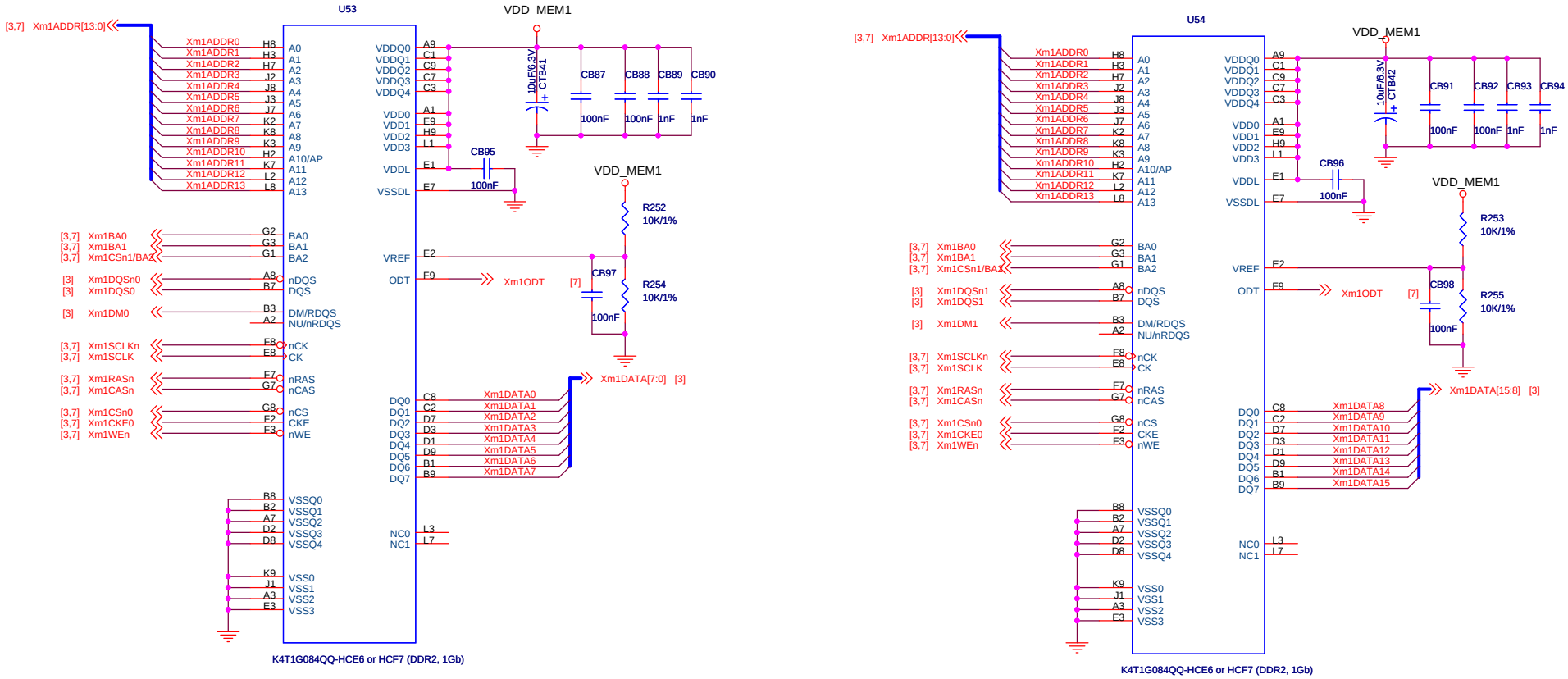
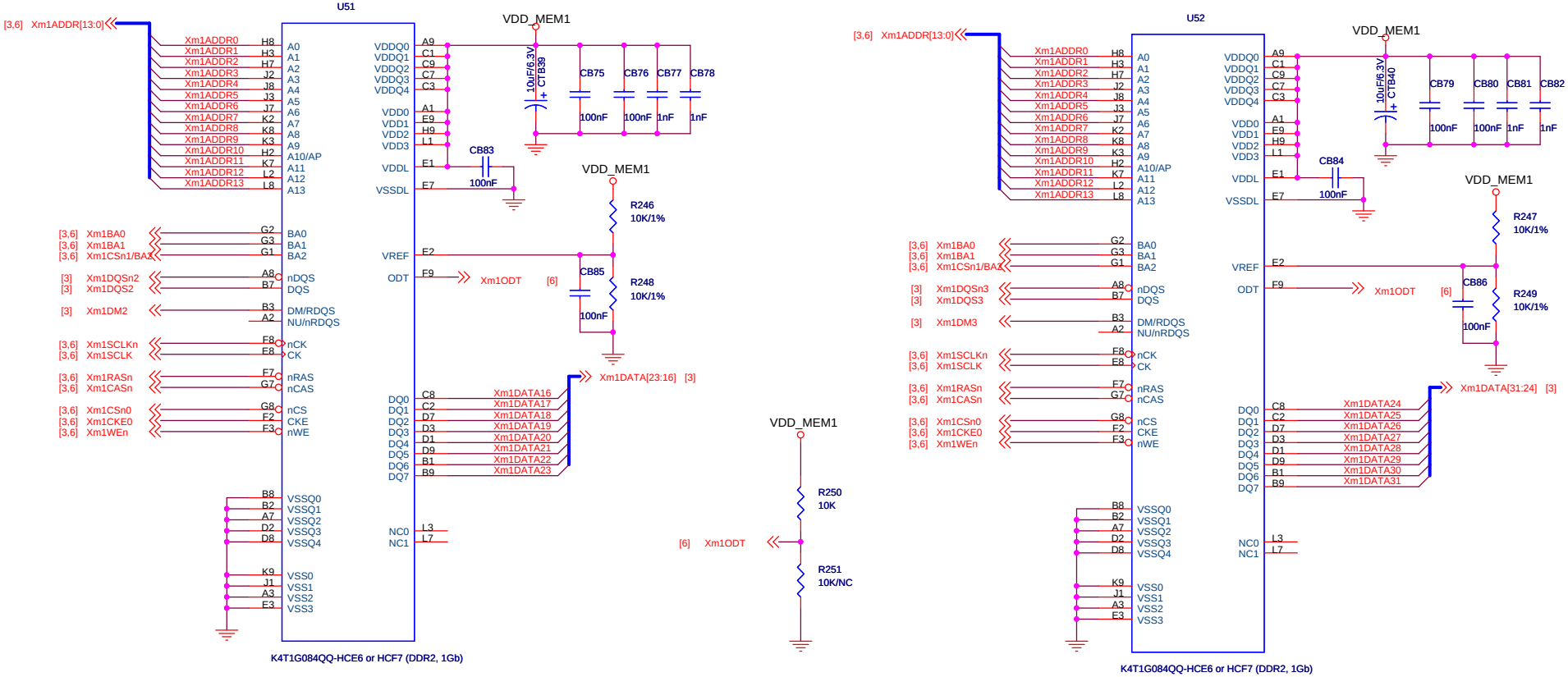


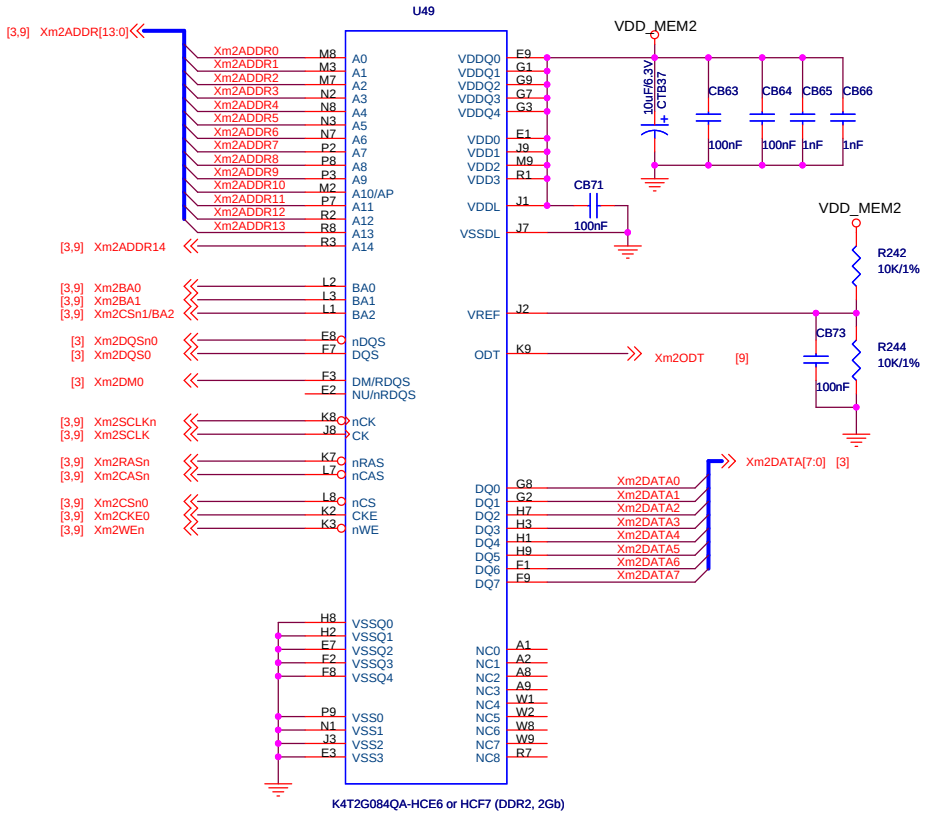
XM1 DDR2(For 1Gbit x8)

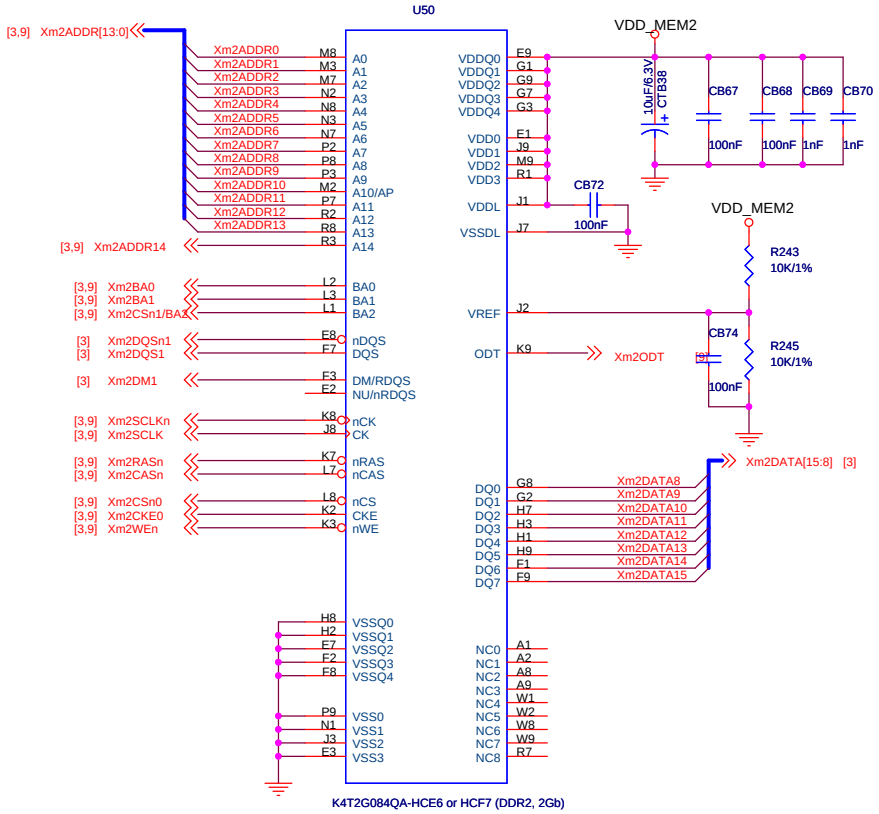
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PV210_POP CPU Board (Evaluation Board)		
Size: A3	Document Number: DDR2(1Gbit*4) XM1 #1,2	Rev: 0.0
Date: Monday, October 26, 2009	Sheet 6 of 21	



XM1 DDR2(For 1Gbit x8)

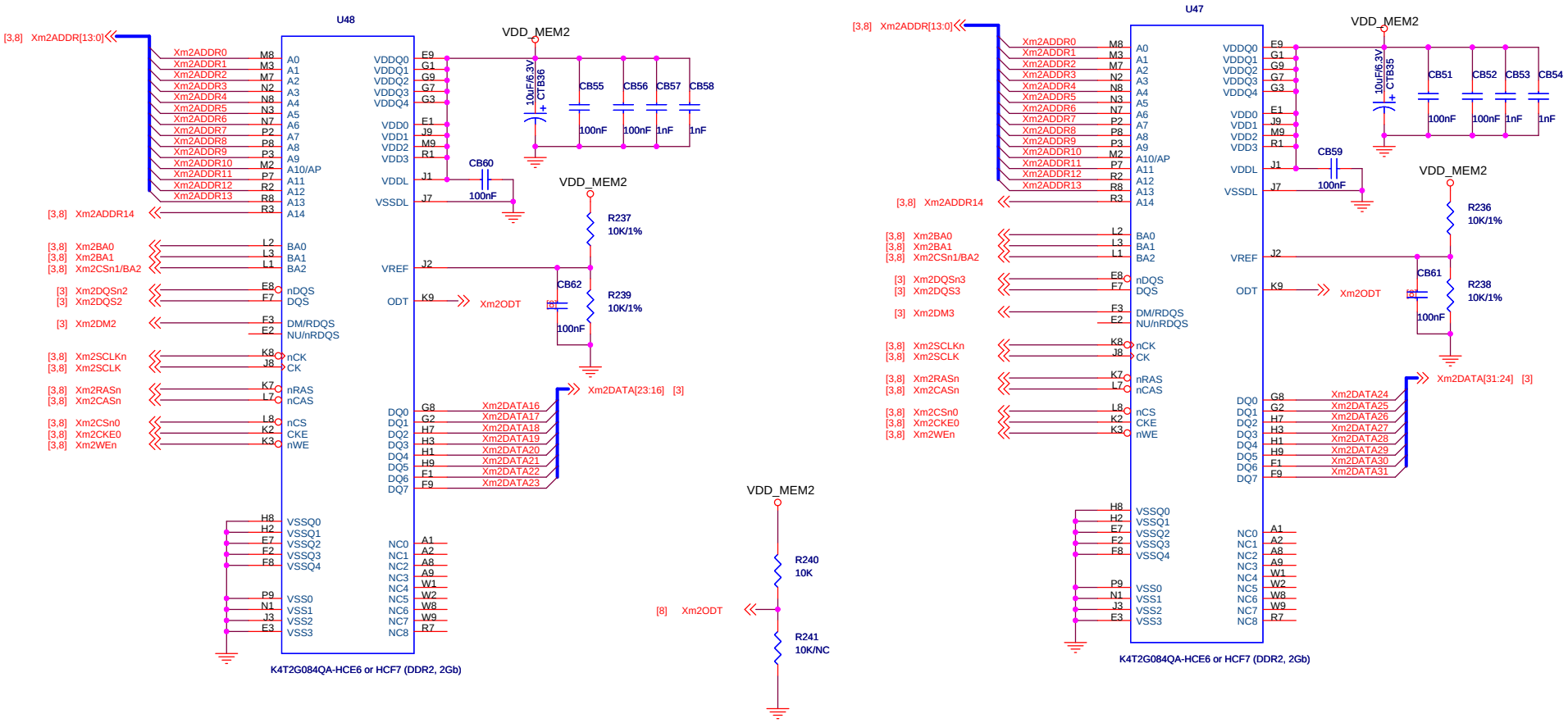
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PV210_CPU Board (Evaluation Board)		
Size: A3	Document Number: DDR2(1Gbit*4) XM1 #2,3	Rev: 0.0
Date: Monday, October 26, 2009	Sheet 7 of 21	





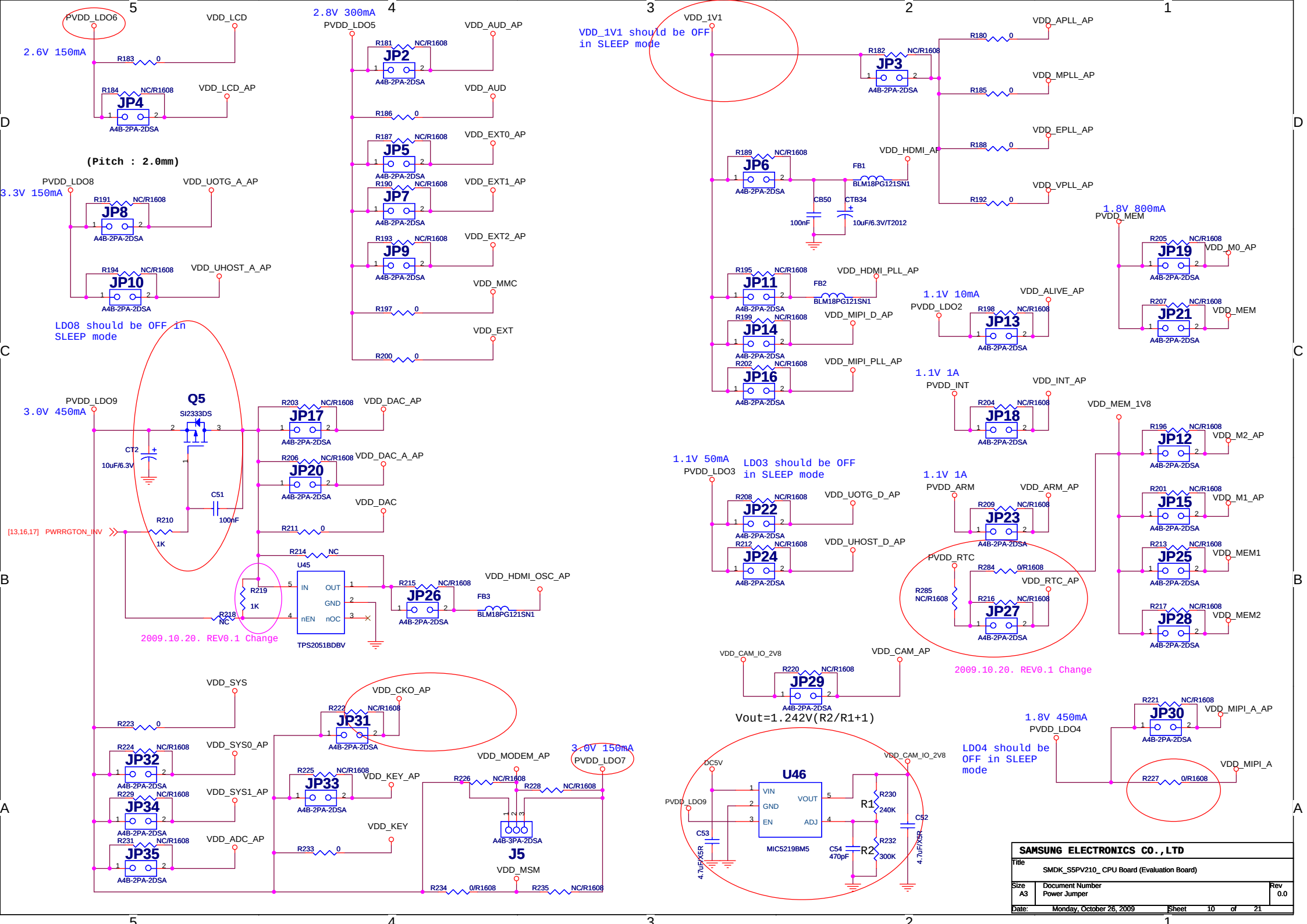
XM2 DDR2(For 2Gbit x8)

SAMSUNG ELECTRONICS CO.,LTD			
Title: SMDK_S5PV210_CPU Board (Evaluation Board)			
Size: A3	Document Number: DDR2(2Gbit*4) XM2 #0,1		Rev: 0.0
Date: Monday, October 26, 2009	Sheet 8 of 21		



XM2 DDR2(For 2Gbit x8)

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PV210_POP CPU Board (Evaluation Board)		
Size: A3	Document Number: DDR2(2Gbit*4) XM2 #2,3	Rev: 0.0
Date: Monday, October 26, 2009	Sheet 9 of 21	


PVDD_LDO6
2.6V 150mA
VDD_LCD
R183 0
R184 NC/R1608
JP4
A4B-2PA-2DSA
VDD_LCD_AP
(Pitch : 2.0mm)
PVDD_LDO8
3.3V 150mA
R191 NC/R1608
JP8
VDD_UOTG_A_AP
R194 NC/R1608
JP10
VDD_UHOST_A_AP
LDO8 should be OFF in SLEEP mode
2.8V 300mA
PVDD_LDO5
R181 NC/R1608
JP2
VDD_AUD_AP
R186 0
VDD_AUD
R187 NC/R1608
JP5
VDD_EXT0_AP
R190 NC/R1608
JP7
VDD_EXT1_AP
R193 NC/R1608
JP9
VDD_EXT2_AP
VDD_MMC
R197 0
VDD_EXT
R200 0
VDD_1V1
VDD_1V1 should be OFF in SLEEP mode
R182 NC/R1608
JP3
VDD_APLL_AP
R180 0
VDD_MPLL_AP
R185 0
VDD_EPLL_AP
R188 0
VDD_VPLL_AP
R192 0
R189 NC/R1608
JP6
FB1
BLM18PG121SN1
VDD_HDMI_AP
CB50 100nF
CTB34 10uF/6.3V/T2012
R195 NC/R1608
JP11
FB2
BLM18PG121SN1
VDD_HDMI_PLL_AP
R199 NC/R1608
JP14
VDD_MIPI_D_AP
R202 NC/R1608
JP16
VDD_MIPI_PLL_AP
1.1V 10mA
PVDD_LDO2
R198 NC/R1608
JP13
VDD_ALIVE_AP
1.8V 800mA
PVDD_MEM
R205 NC/R1608
JP19
VDD_M0_AP
R207 NC/R1608
JP21
VDD_MEM
1.1V 1A
PVDD_INT
R204 NC/R1608
JP18
VDD_INT_AP
PVDD_LDO9
3.0V 450mA
Q5
SI2333DS
CT2 10uF/6.3V
C51 100nF
R210 1K
[13,16,17] PWRRGTON_INV
R203 NC/R1608
JP17
VDD_DAC_AP
R206 NC/R1608
JP20
VDD_DAC_A_AP
VDD_DAC
R211 0
R214 NC
U45
TPS2051BDBV
IN OUT GND nEN nOC
R219 1K
R218 NC
R215 NC/R1608
JP26
FB3
BLM18PG121SN1
VDD_HDMI_OSC_AP
2009.10.20. REV0.1 Change
1.1V 50mA
PVDD_LDO3
LDO3 should be OFF in SLEEP mode
R208 NC/R1608
JP22
VDD_UOTG_D_AP
R212 NC/R1608
JP24
VDD_UHOST_D_AP
1.1V 1A
PVDD_ARM
R209 NC/R1608
JP23
VDD_ARM_AP
PVDD_RTC
R284 0/R1608
VDD_RTC_AP
R285 NC/R1608
R216 NC/R1608
JP27
2009.10.20. REV0.1 Change
VDD_MEM_1V8
R196 NC/R1608
JP12
VDD_M2_AP
R201 NC/R1608
JP15
VDD_M1_AP
R213 NC/R1608
JP25
VDD_MEM1
R217 NC/R1608
JP28
VDD_MEM2
VDD_CAM_IO_2V8
R220 NC/R1608
JP29
VDD_CAM_AP
Vout=1.242V(R2/R1+1)
1.8V 450mA
PVDD_LDO4
LDO4 should be OFF in SLEEP mode
R221 NC/R1608
JP30
VDD_MIPI_A_AP
R227 0/R1608
VDD_MIPI_A
VDD_SYS
R223 0
VDD_CKO_AP
R222 NC/R1608
JP31
VDD_SYS0_AP
R224 NC/R1608
JP32
VDD_SYS1_AP
R229 NC/R1608
JP34
VDD_ADC_AP
R231 NC/R1608
JP35
VDD_KEY_AP
R225 NC/R1608
JP33
VDD_KEY
R233 0
3.0V 150mA
PVDD_LDO7
VDD_MODEM_AP
R226 NC/R1608
R228 NC/R1608
A4B-3PA-2DSA
J5
VDD_MSM
R234 0/R1608
R235 NC/R1608
DC5V
PVDD_LDO9
U46
MIC5219BM5
VIN GND EN VOUT ADJ
C53 4.7uF/X5R
C54 470pF
R1 240K
R2 300K
R230
R232
C52 4.7uF/X5R
VDD_CAM_IO_2V8
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK_S5PV210_ CPU Board (Evaluation Board)
Size A3
Document Number
Power Jumper
Rev 0.0
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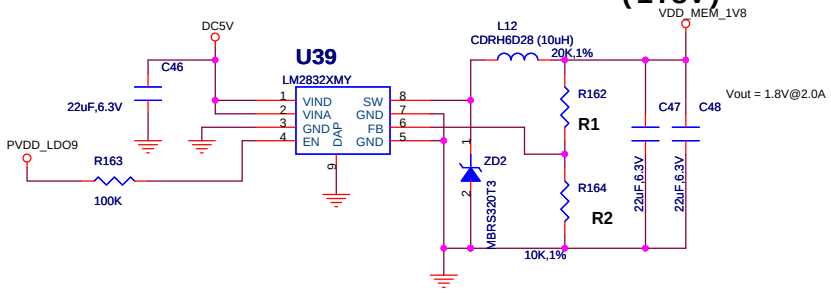
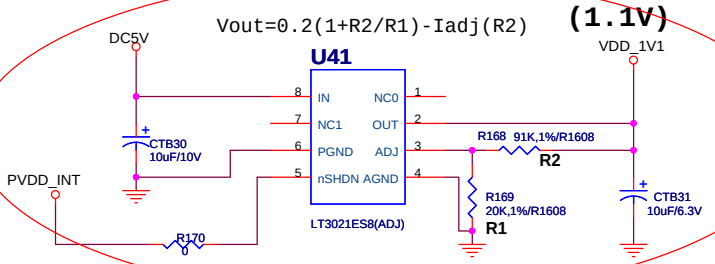
Vout=0.60(1+R1/R2)
R1=R2(Vout/0.60V-1)

(1.8V)



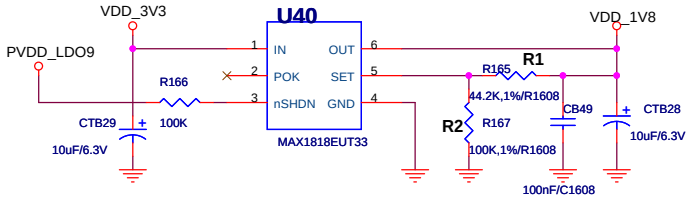
Vout=0.2(1+R2/R1)-Iadj(R2)

(1.1V)



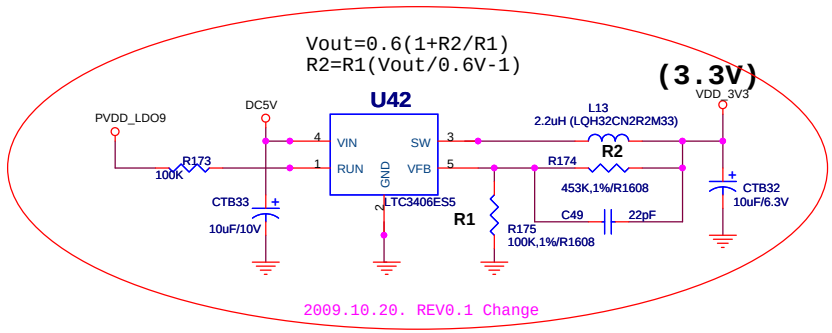
Vout=1.25(1+R1/R2)
R1=R2(Vout/1.25V-1)

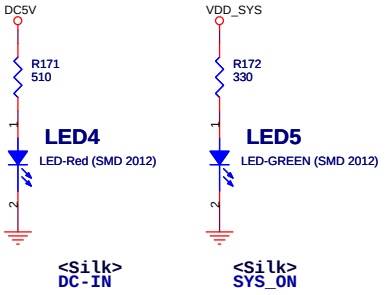
(1.8V)

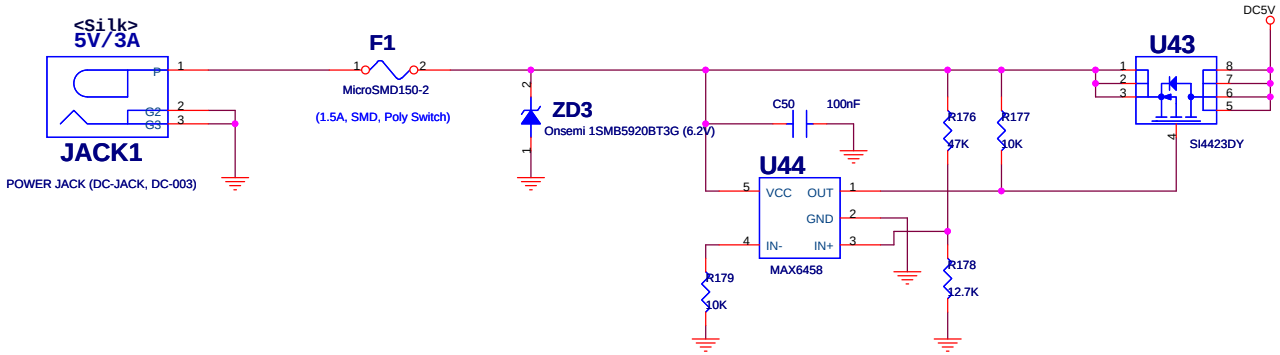


Vout=0.6(1+R2/R1)
R2=R1(Vout/0.6V-1)

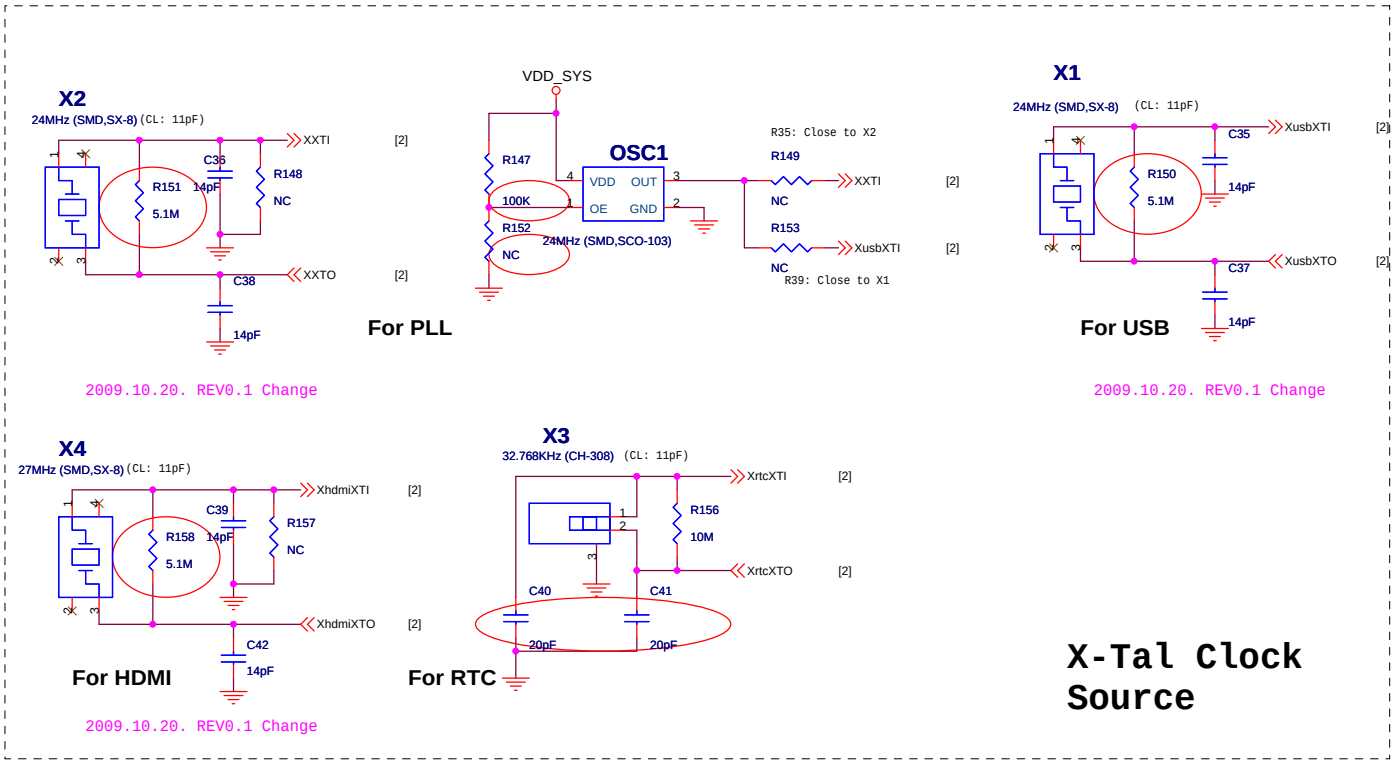
(3.3V)

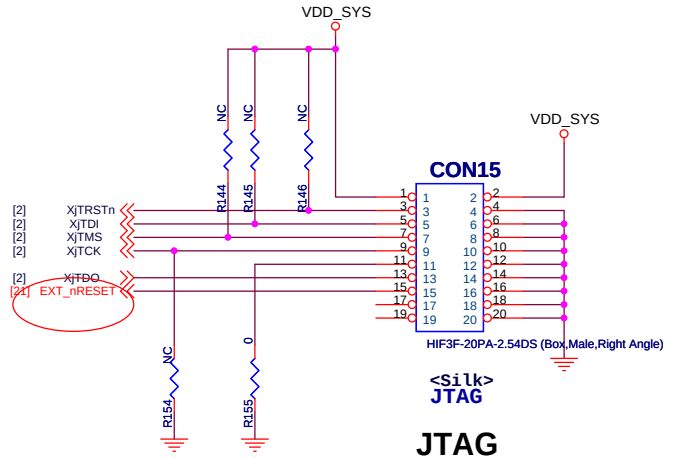




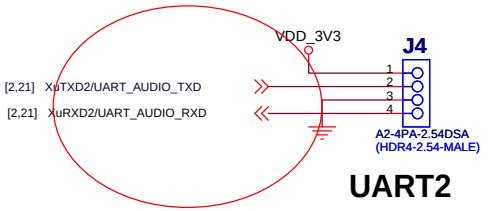


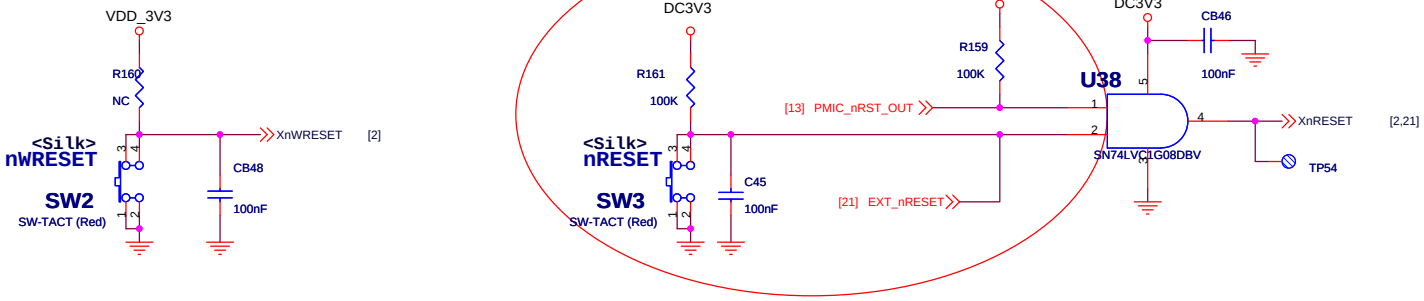
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PV210_CPU Board (Evaluation Board)		
Size: A3	Document Number: Power(DCjack&Regulator)	Rev: 0.0
Date: Monday, October 26, 2009	Sheet 11 of 21	

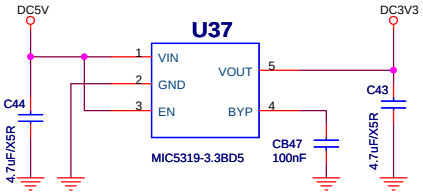




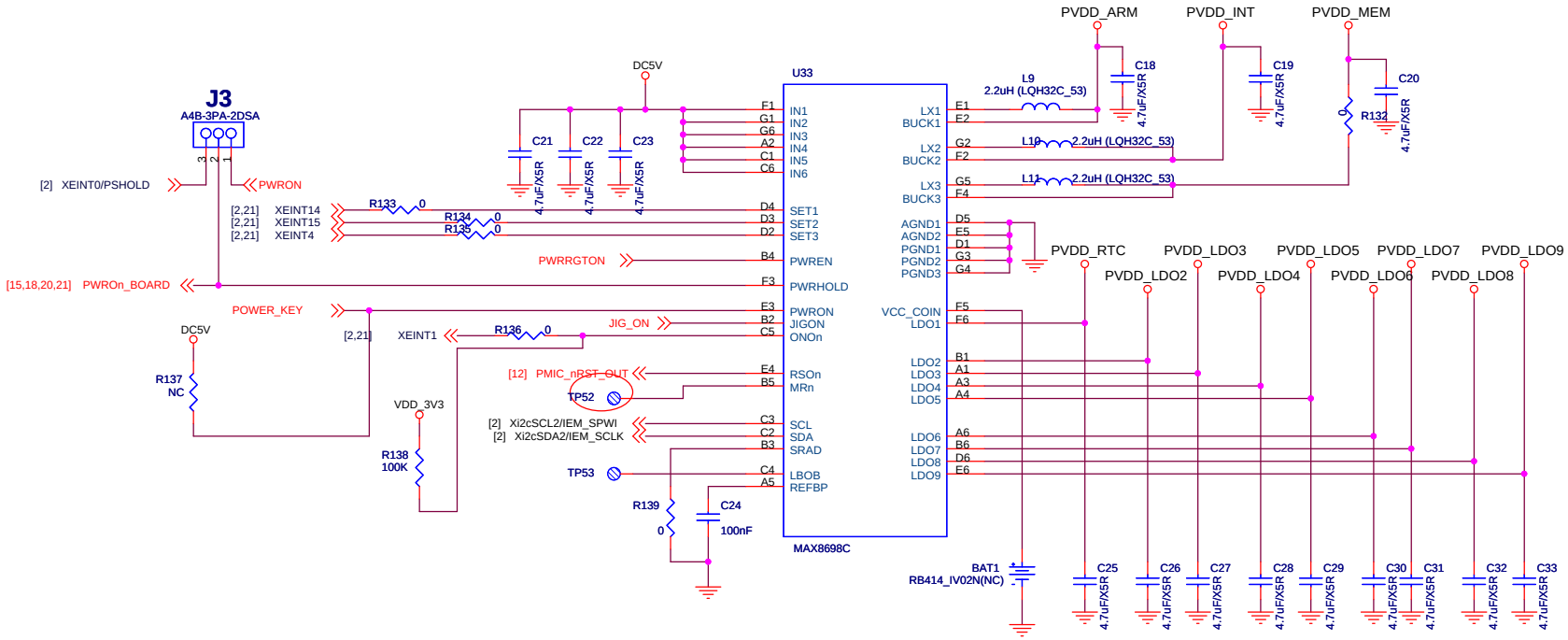
*Pull-up, Pull-down resistors are embeded

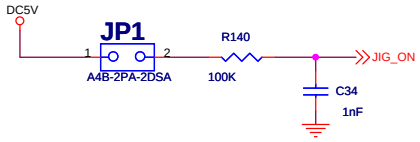


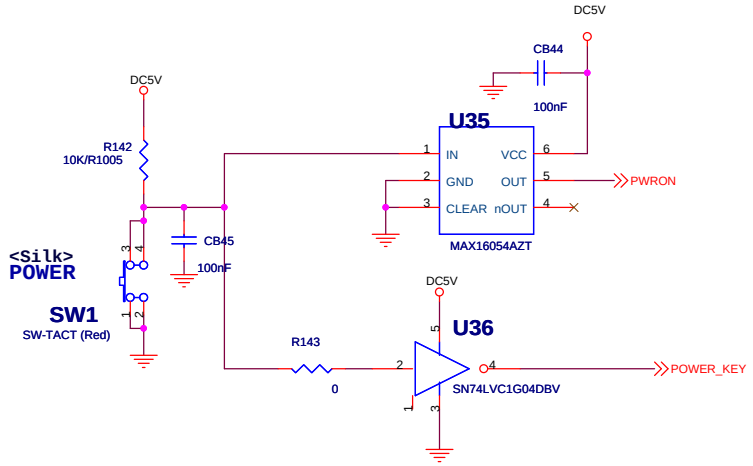


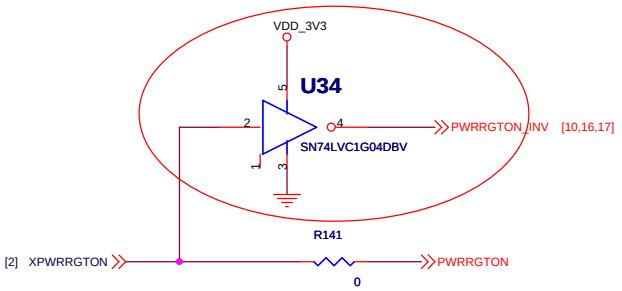


SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PV210_POP CPU Board (Evaluation Board)		
Size: A3	Document Number: Reset / Clock source / JTAG	Rev: 0.0
Date: Monday, October 26, 2009	Sheet 12 of 21	

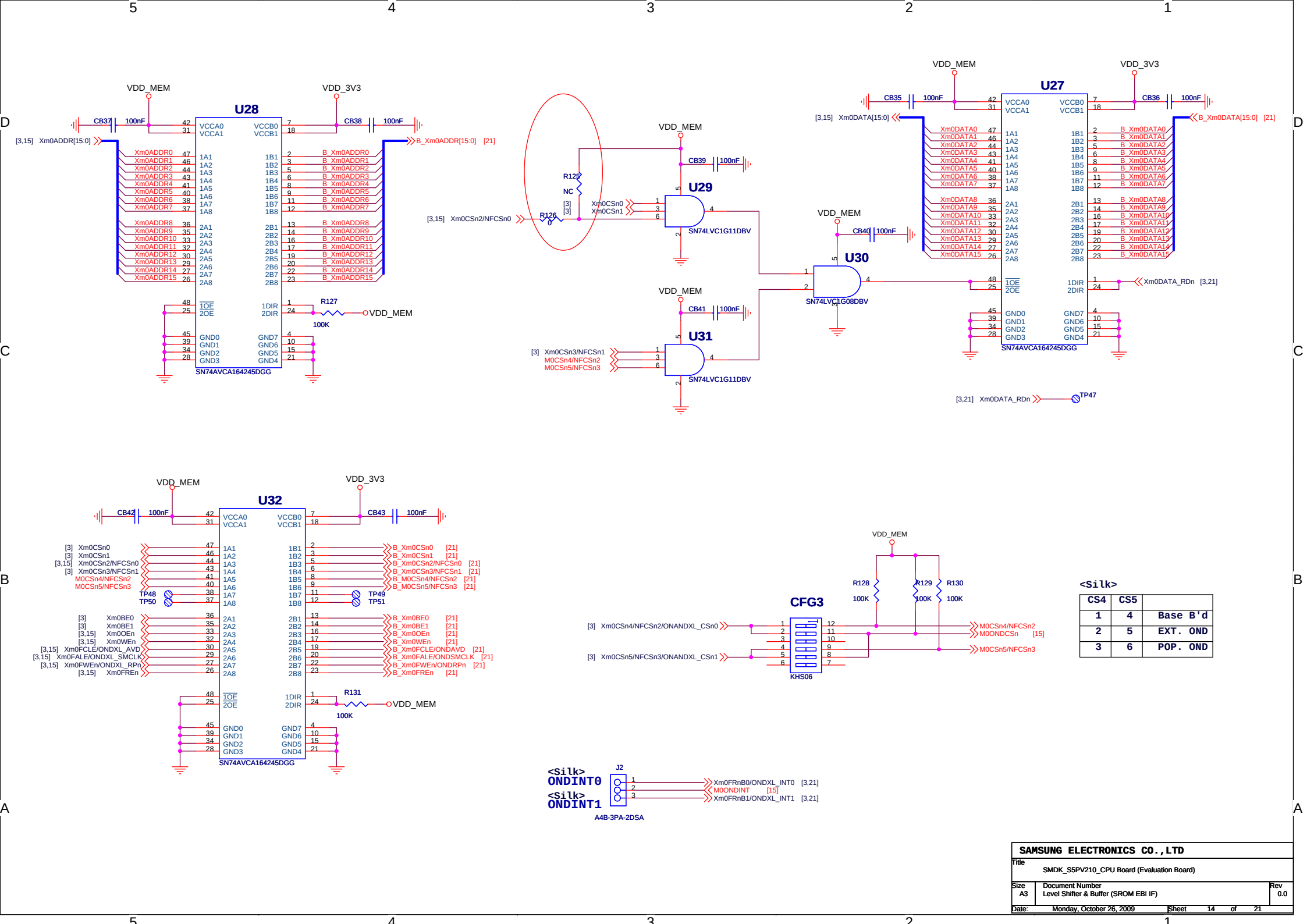








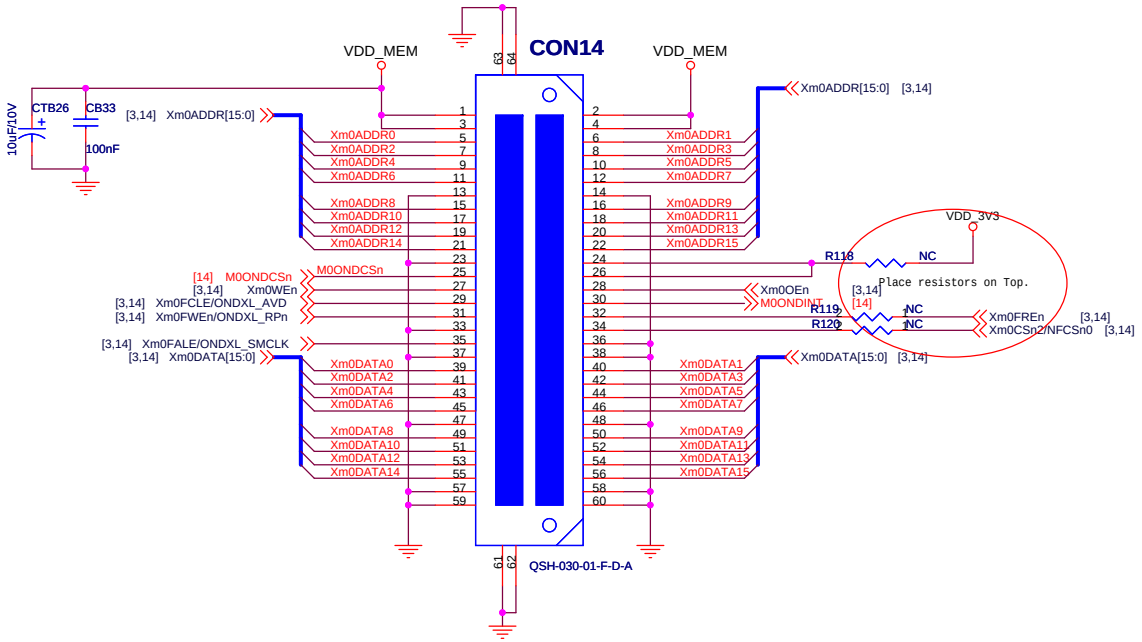
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PV210_CPU Board (Evaluation Board)		
Size: A3	Document Number: Power - PMIC Socket	Rev: 0.0
Date: Monday, October 26, 2009	Sheet 13 of 21	



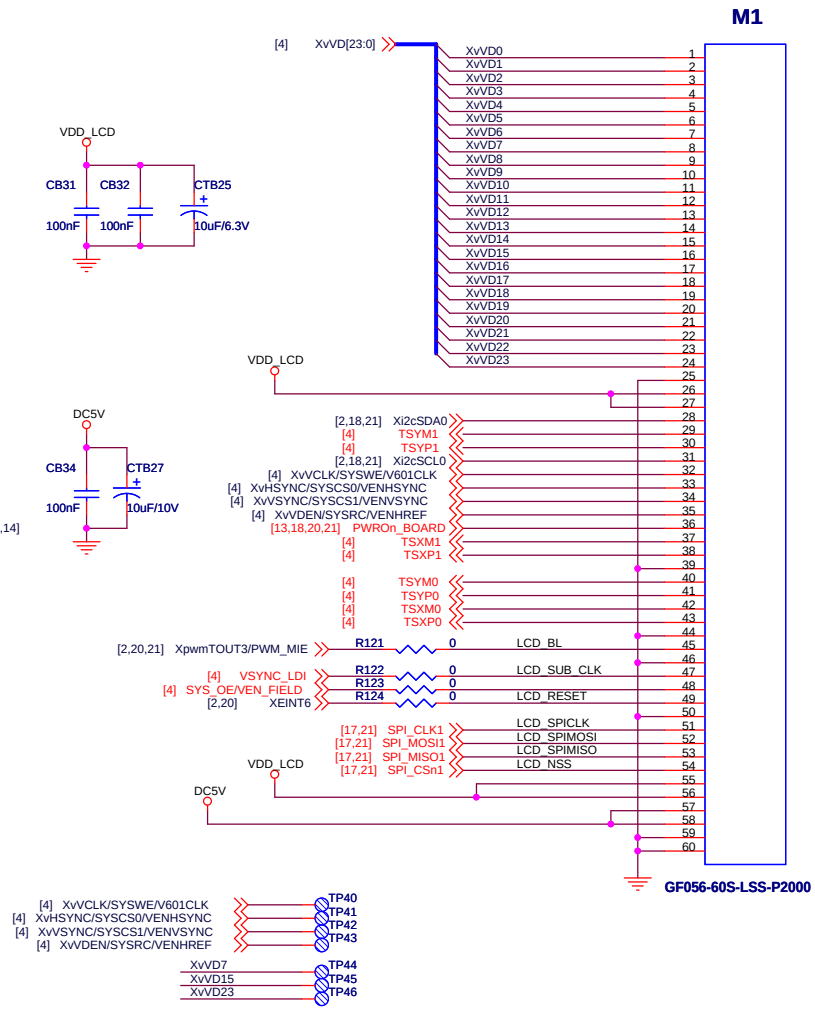
CS4	CS5	
1	4	Base B'd
2	5	EXT. OND
3	6	POP. OND

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PV210_CPU Board (Evaluation Board)		
Size: A3	Document Number: Level Shifter & Buffer (SROM EBI IF)	Rev: 0.0
Date: Monday, October 26, 2009	Sheet 14 of 21	

OneNAND Connector



TFT LCD FPC Cable Interface
(MODULE Board)



SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PV210_CPU Board (Evaluation Board)		
Size: A3	Document Number: OneNAND / LCD I/F(NonMIPI)	Rev: 0.0
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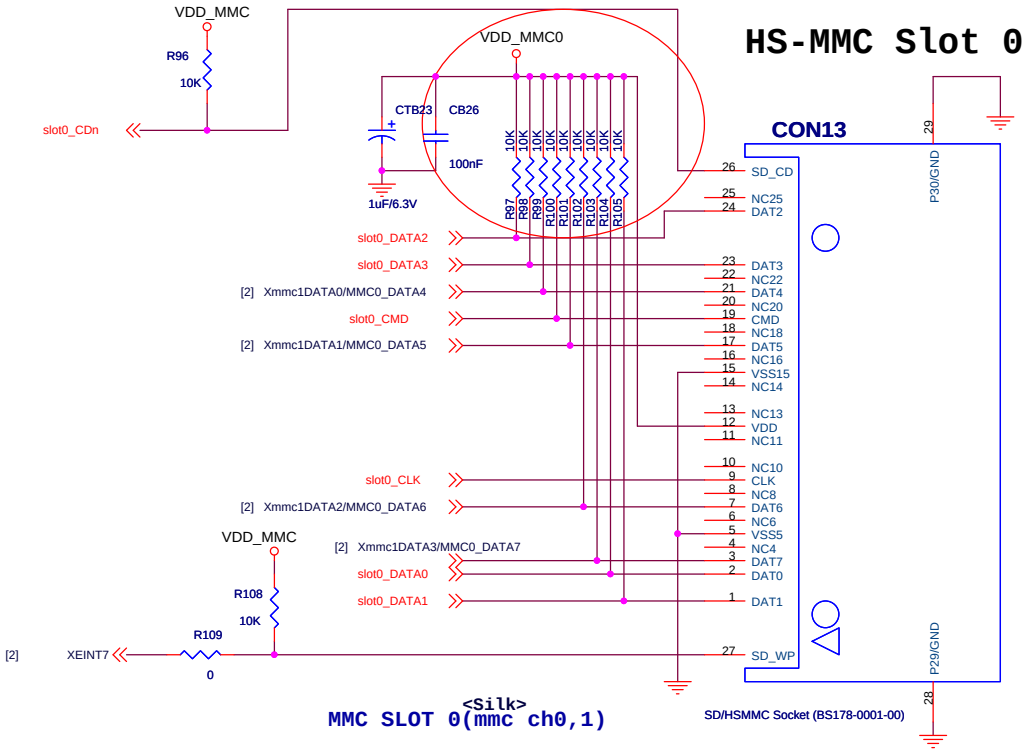
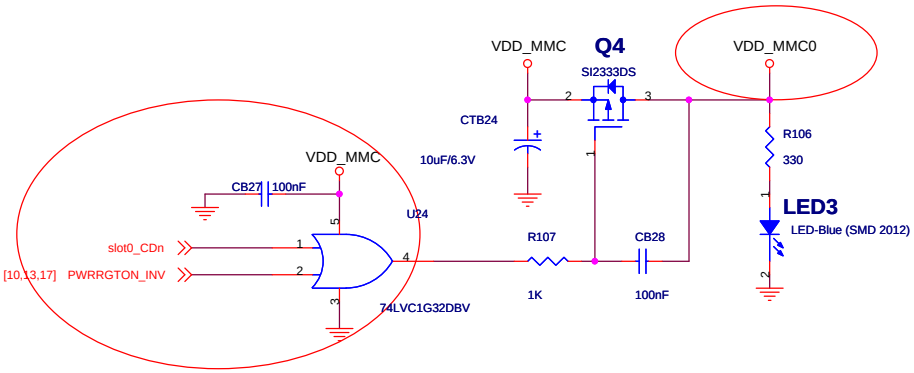
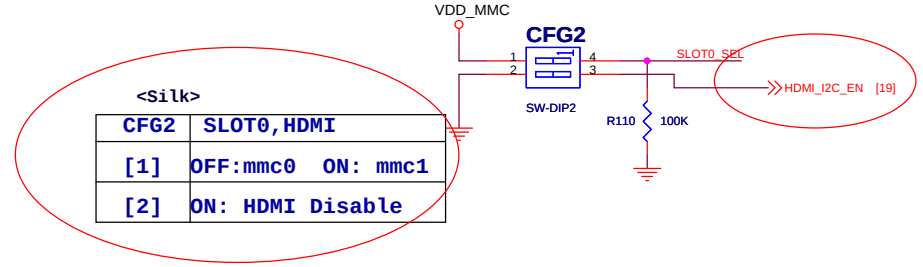
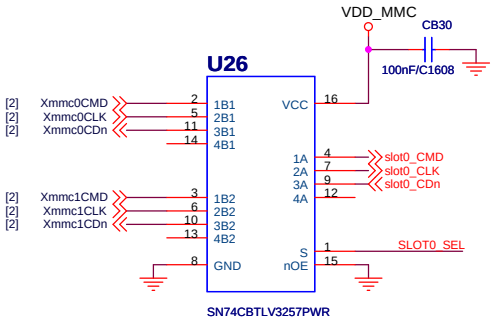
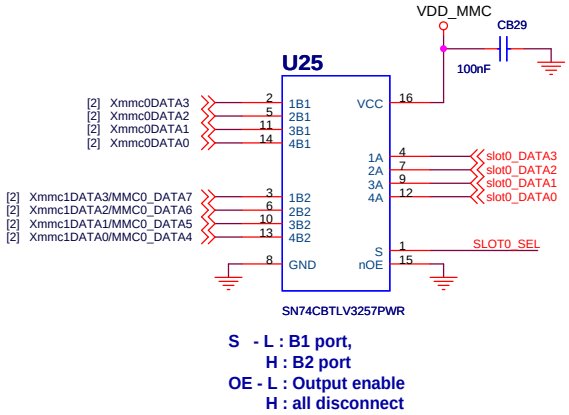
HS-MMC Slot 0



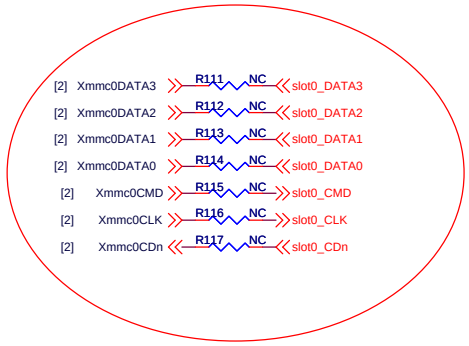




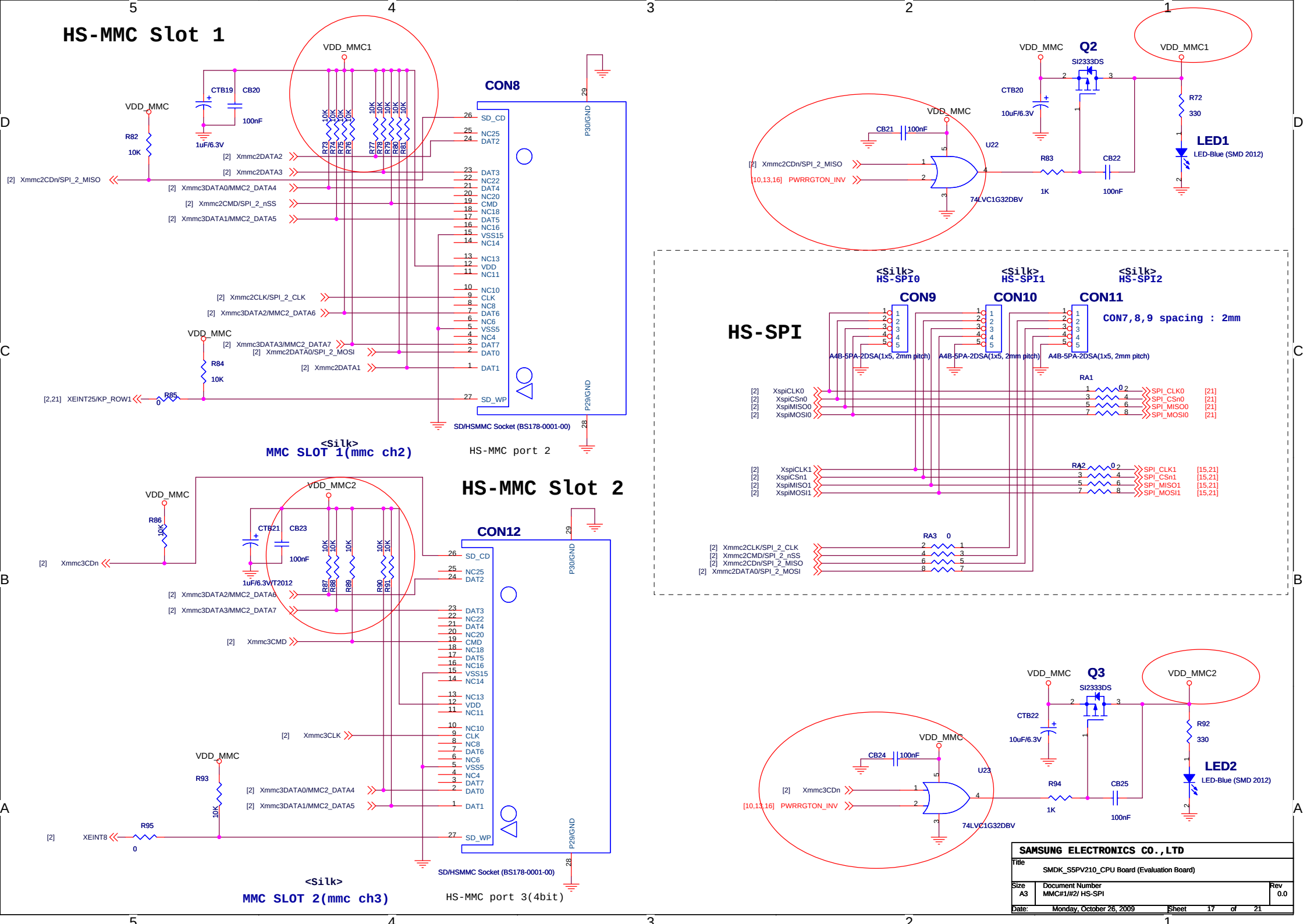




S - L : B1 port,
H : B2 port
OE - L : Output enable
H : all disconnect



SAMSUNG ELECTRONICS CO.,LTD	
Title: SMDK_S5PV210_CPU Board (Evaluation Board)	
Size: A3	Document Number: MMC#0 — Rev: 0.0
Date: Monday, October 26, 2009	Sheet 16 of 21


HS-MMC Slot 1
VDD_MMC1
CON8
CTB19
CB20
100nF
1uF/6.3V
VDD_MMC
R82
10K
[2] Xmmc2CDn/SPI_2_MISO
[2] Xmmc2DATA2
[2] Xmmc2DATA3
[2] Xmmc3DATA0/MMC2_DATA4
[2] Xmmc2CMD/SPI_2_nSS
[2] Xmmc3DATA1/MMC2_DATA5
[2] Xmmc2CLK/SPI_2_CLK
[2] Xmmc3DATA2/MMC2_DATA6
[2] Xmmc3DATA3/MMC2_DATA7
[2] Xmmc2DATA0/SPI_2_MOSI
[2] Xmmc2DATA1
R84
10K
[2,21] XEINT25/KP_ROW1
R85
0
SD_CD
NC25
DAT2
DAT3
NC22
DAT4
NC20
CMD
NC18
DAT5
NC16
VSS15
NC14
NC13
VDD
NC11
NC10
CLK
NC8
DAT6
NC6
VSS5
NC4
DAT7
DAT0
DAT1
SD_WP
P30/GND
P29/GND
SD/HSMMC Socket (BS178-0001-00)
<Silk>
MMC SLOT 1(mmc ch2)
HS-MMC port 2
HS-MMC Slot 2
VDD_MMC2
CON12
CTB21
CB23
100nF
1uF/6.3V/T2012
VDD_MMC
R86
10K
[2] Xmmc3CDn
[2] Xmmc3DATA2/MMC2_DATA6
[2] Xmmc3DATA3/MMC2_DATA7
[2] Xmmc3CMD
[2] Xmmc3CLK
[2] Xmmc3DATA0/MMC2_DATA4
[2] Xmmc3DATA1/MMC2_DATA5
R93
10K
[2] XEINT8
R95
0
<Silk>
MMC SLOT 2(mmc ch3)
HS-MMC port 3(4bit)
VDD_MMC
Q2
SI2333DS
VDD_MMC1
CTB20
10uF/6.3V
CB21
100nF
U22
[2] Xmmc2CDn/SPI_2_MISO
[10,13,16] PWRRGTON_INV
74LVC1G32DBV
R83
1K
CB22
100nF
R72
330
LED1
LED-Blue (SMD 2012)
HS-SPI
<Silk>
HS-SPI0
<Silk>
HS-SPI1
<Silk>
HS-SPI2
CON9
CON10
CON11
CON7,8,9 spacing : 2mm
A4B-5PA-2DSA(1x5, 2mm pitch)
RA1
RA2
RA3
[2] XspiCLK0
[2] XspiCSn0
[2] XspiMISO0
[2] XspiMOSI0
[2] XspiCLK1
[2] XspiCSn1
[2] XspiMISO1
[2] XspiMOSI1
[2] Xmmc2CLK/SPI_2_CLK
[2] Xmmc2CMD/SPI_2_nSS
[2] Xmmc2CDn/SPI_2_MISO
[2] Xmmc2DATA0/SPI_2_MOSI
SPI_CLK0 [21]
SPI_CSn0 [21]
SPI_MISO0 [21]
SPI_MOSI0 [21]
SPI_CLK1 [15,21]
SPI_CSn1 [15,21]
SPI_MISO1 [15,21]
SPI_MOSI1 [15,21]
VDD_MMC
Q3
SI2333DS
VDD_MMC2
CTB22
10uF/6.3V
CB24
100nF
U23
[2] Xmmc3CDn
[10,13,16] PWRRGTON_INV
74LVC1G32DBV
R94
1K
CB25
100nF
R92
330
LED2
LED-Blue (SMD 2012)
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK_S5PV210_CPU Board (Evaluation Board)
Size
A3
Document Number
MMC#1/#2/ HS-SPI
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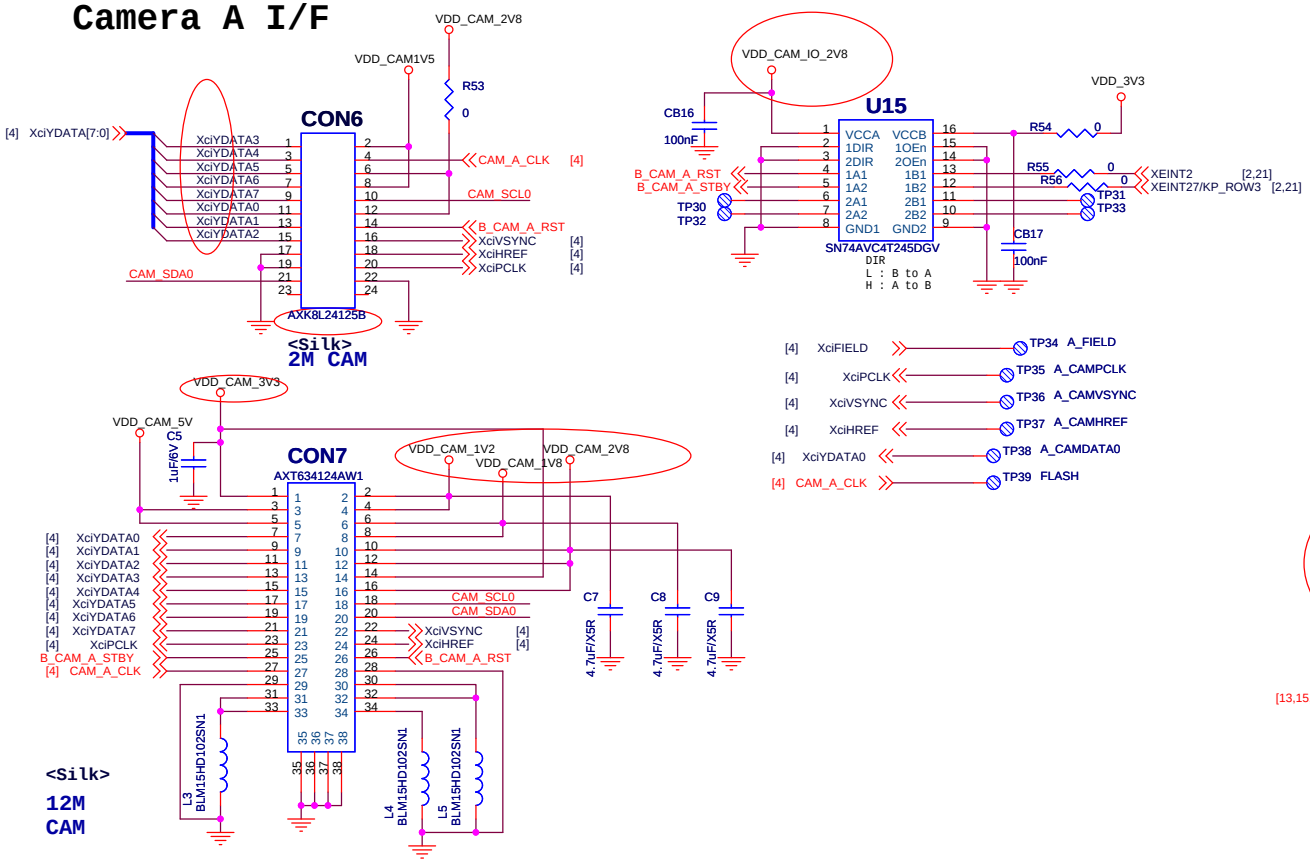
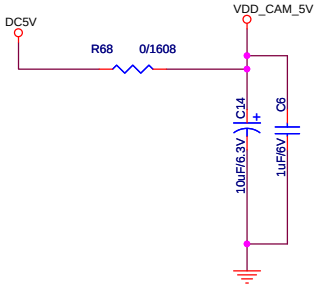
Camera A I/F



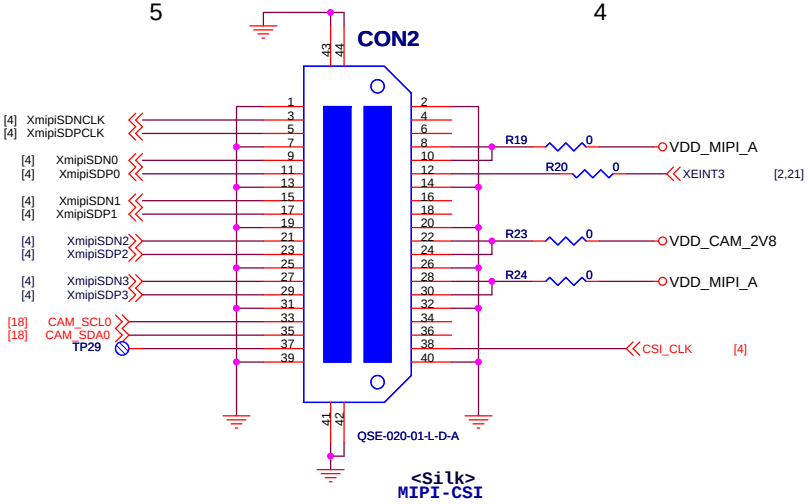
Power for CAM

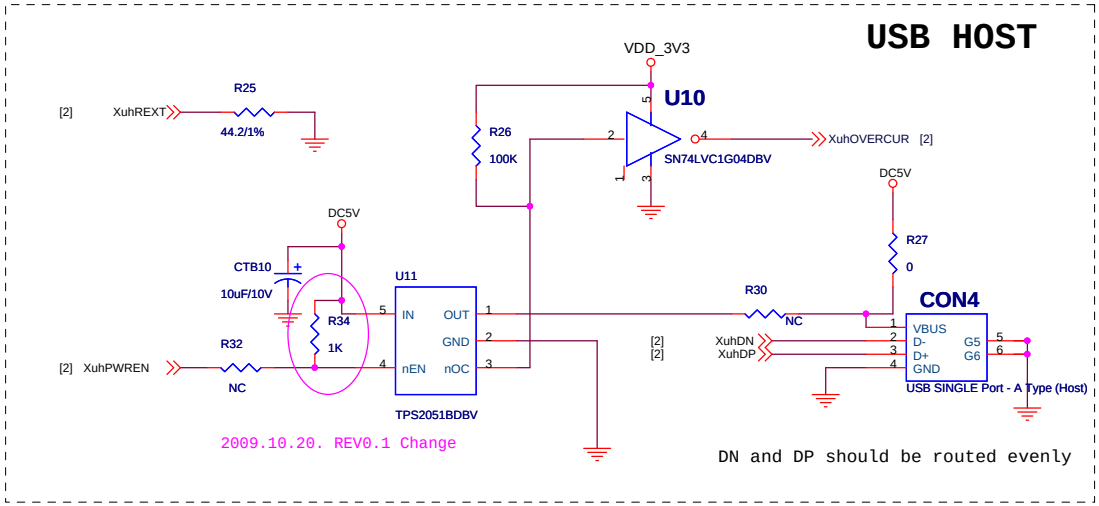


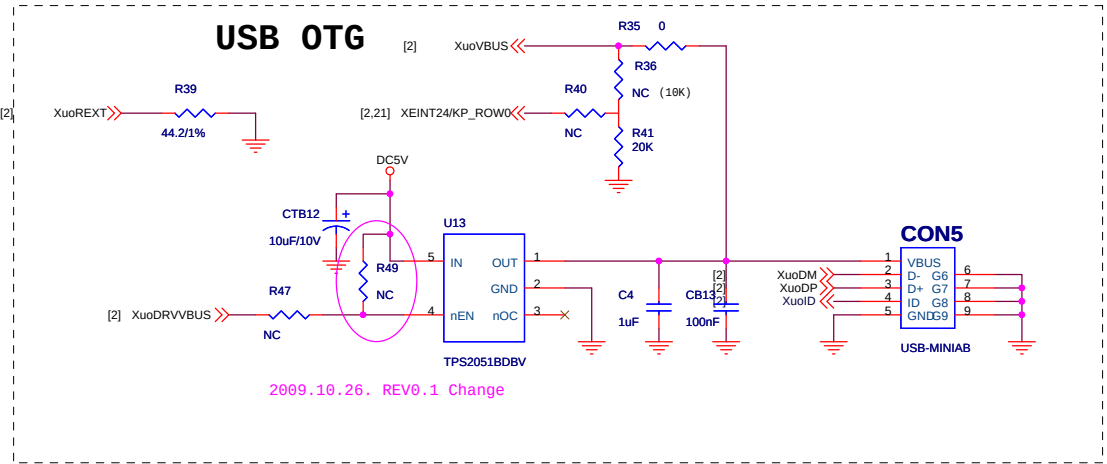
2009.10.20. REV0.1 Change

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PV210_CPU Board (Evaluation Board)		
Size: A3	Document Number: MMC#1 / HS-SPI / Camera I/F A Port(Non-MIPI)	Rev: 0.0
Date: Monday, October 26, 2009	Sheet 18 of 21	

MIPI-CSI Camera Module Interface

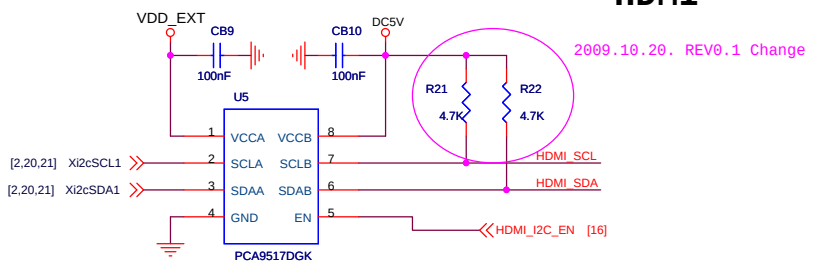


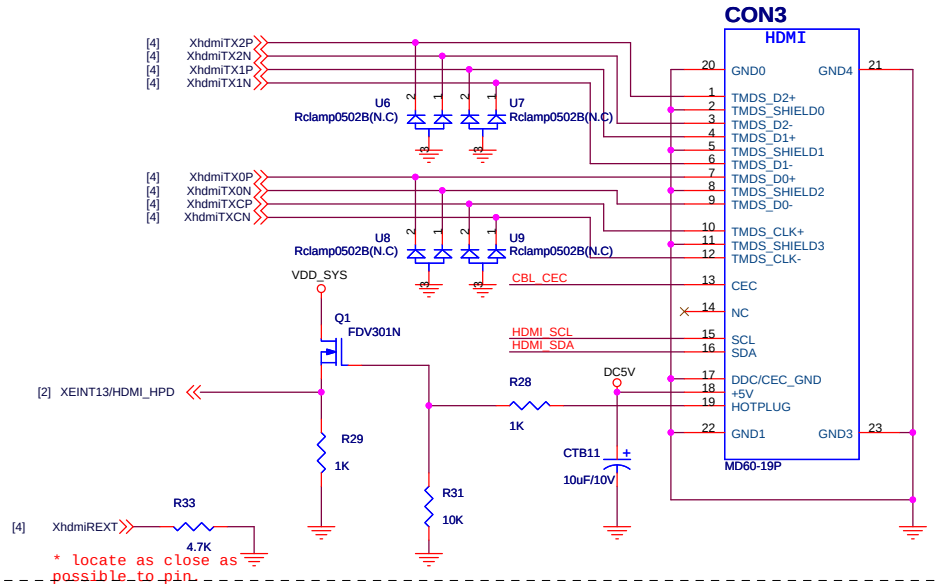


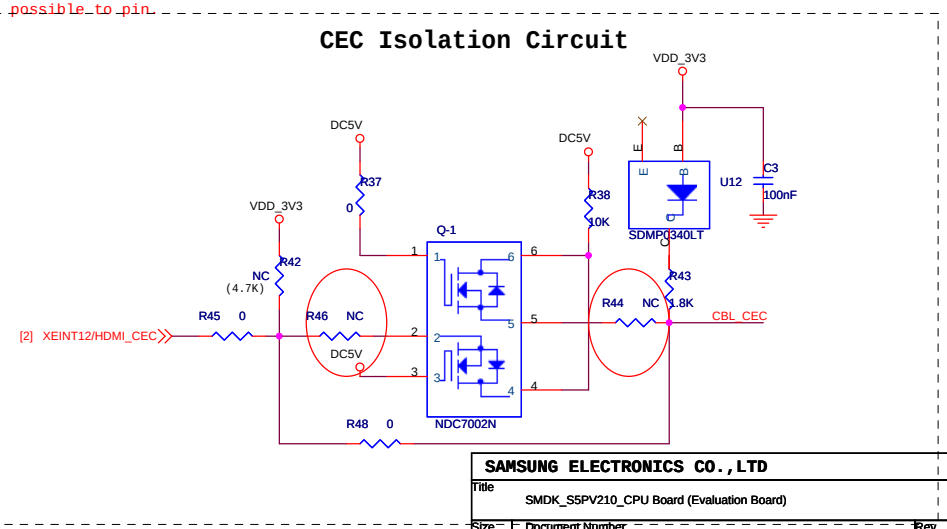


Signal Name, Power Domain matching 필요

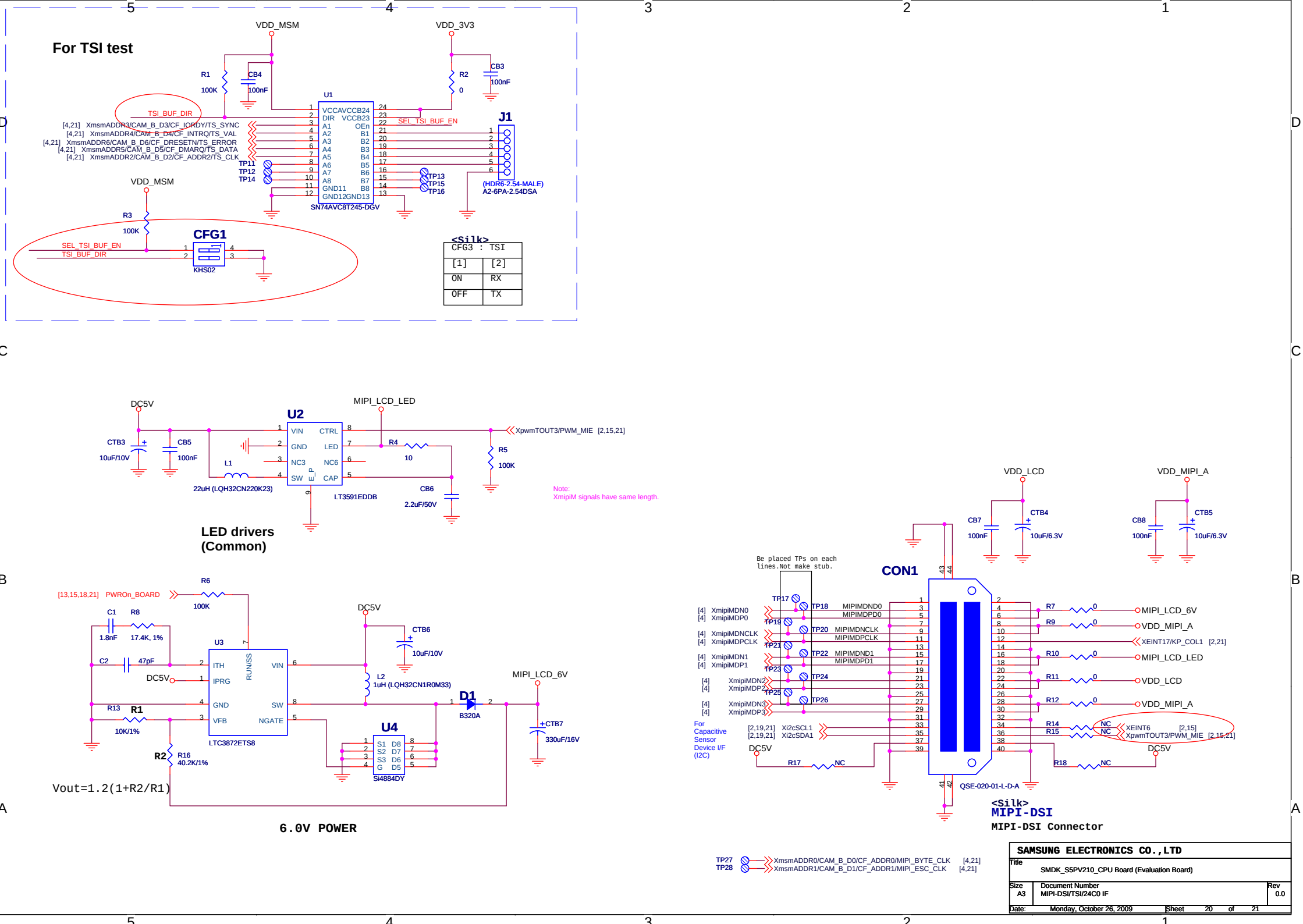
HDMI







SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PV210_CPU Board (Evaluation Board)		
Size: A3	Document Number: HDMI/ MIPI-CSI/ MIPI-HSI/ USB	Rev: 0.0
Date: Monday, October 26, 2009	Sheet 19 of 21	



SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PV210_CPU Board (Evaluation Board)		
Size: A3	Document Number: MIPI-DSI/TSI/24C0 IF	Rev: 0.0
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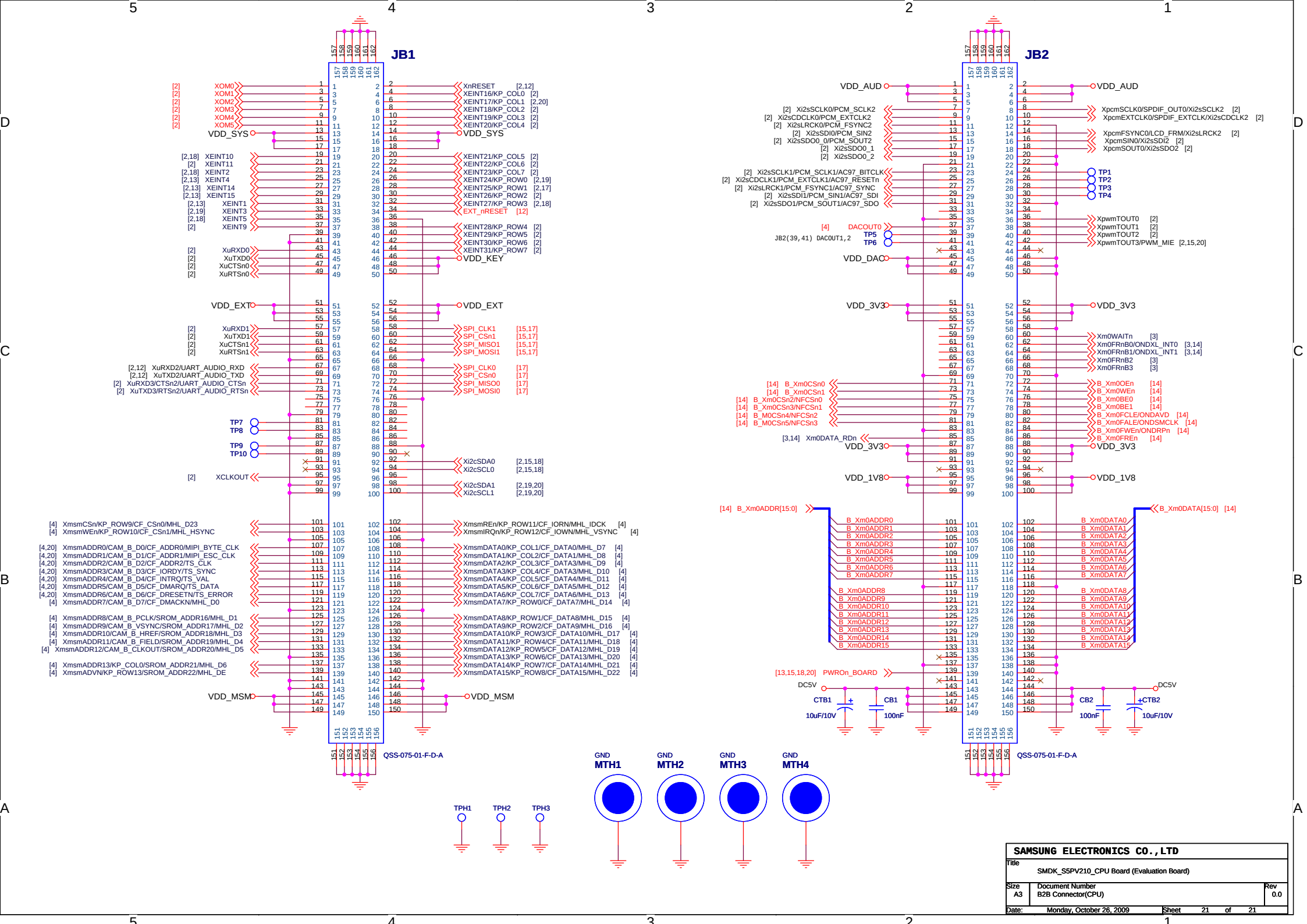
JB1
JB2
QSS-075-01-F-D-A
VDD_SYS
VDD_KEY
VDD_EXT
VDD_MSM
VDD_AUD
VDD_DAC
VDD_3V3
VDD_1V8
XOM0
XOM1
XOM2
XOM3
XOM4
XOM5
XnRESET
EXT_nRESET
XCLKOUT
DACOUT0
Xm0DATA_RDn
PWROn_BOARD
DC5V
CTB1
10uF/10V
CB1
100nF
CB2
+CTB2
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TPH1
TPH2
TPH3
GND
MTH1
MTH2
MTH3
MTH4
SAMSUNG ELECTRONICS CO.,LTD
SMDK_S5PV210_CPU Board (Evaluation Board)
B2B Connector(CPU)
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SMDK_S5PC110_Base B'd (S5PC110 Evaluation Board) Schematics

Revision	Date	Description
Rev 0.0	2009. 04.	Preliminary Version
Rev 0.1	2009. 08.	

Table of Contents

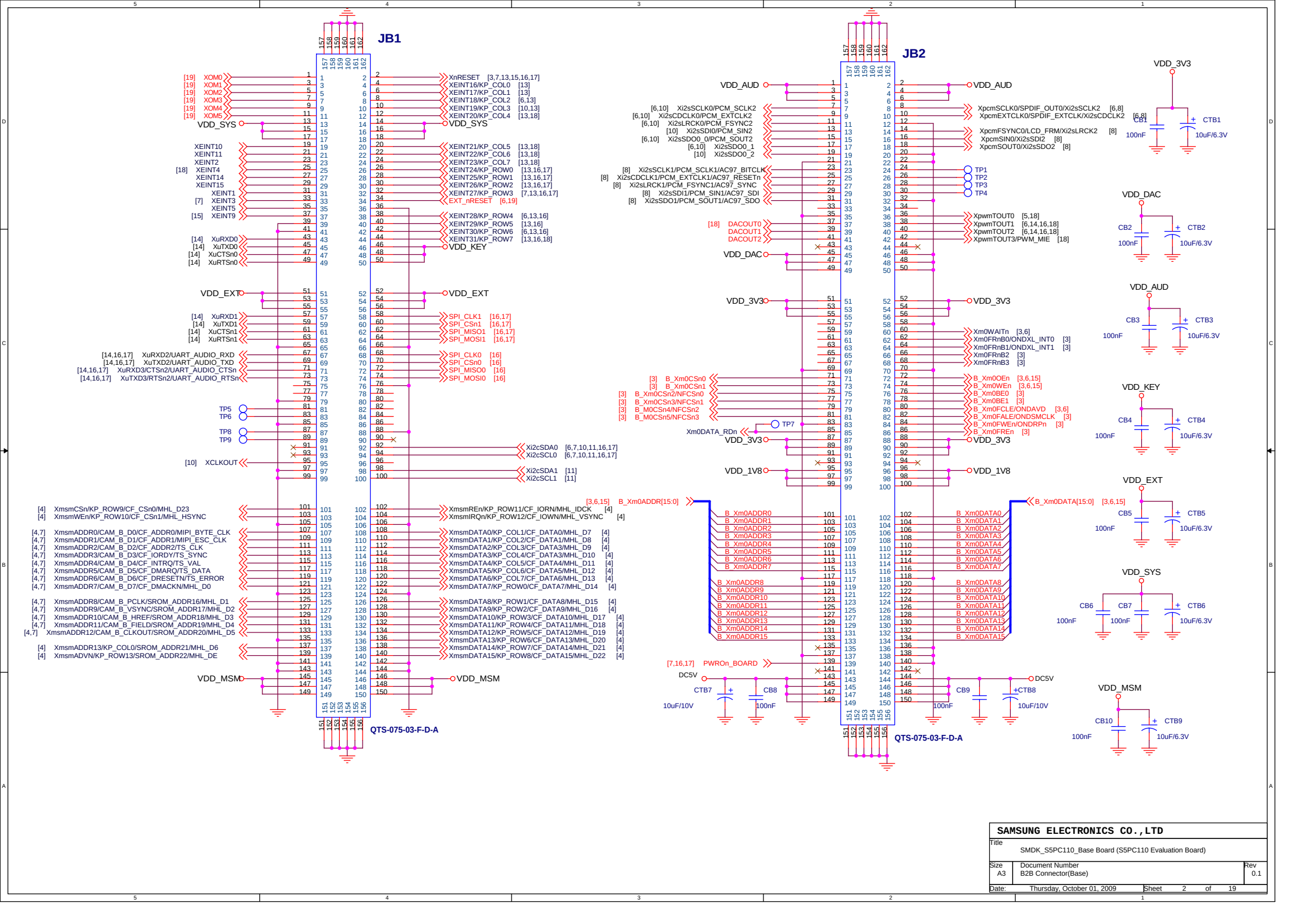
Part Reference

<Component><Number>

U : Component or Regurator IC
C : Capacitor
CB : Capacitor Bypass
CT : Capacitor Tantal
CTB : Capacitor Tantal Bypass
J : Jumper
JB : CPU To Base connector
JP : Jumper Power
R : Resistor
RA : Resistor Array
RP : Resistor Power
VR : Variable Resistor
L : Inductor
FB : Ferrite Bead
OSC : Oscillator
X : X-tal (Crystal)
Q : Transistor or FET
D : Diode
ZD : Zener Diode
LED : LED Diode
SW : SWitch Tact/Push
CON : CONnector
CFGB : ConFiGure switch on Baseb'd(DIP/Slide)
TP : Test Point (SMD)
TPH : Test Point Hole (Through Hole)
MTH: Mount Through Hole
M (MOD) : MODule Interface connector

SAMSUNG ELECTRONICS CO.,LTD

Title	SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)	
Size A3	Document Number Revision History	Rev 0.1
Date: Thursday, October 01, 2009	Sheet 1 of 19	


JB1
JB2
QTS-075-03-F-D-A
QTS-075-03-F-D-A
VDD_SYS
VDD_KEY
VDD_EXT
VDD_MSM
VDD_AUD
VDD_DAC
VDD_3V3
VDD_1V8
XnRESET [3,7,13,15,16,17]
XEINT16/KP_COL0 [13]
XEINT17/KP_COL1 [13]
XEINT18/KP_COL2 [6,13]
XEINT19/KP_COL3 [10,13]
XEINT20/KP_COL4 [13,18]
XEINT21/KP_COL5 [13,18]
XEINT22/KP_COL6 [13,18]
XEINT23/KP_COL7 [13,18]
XEINT24/KP_ROW0 [13,16,17]
XEINT25/KP_ROW1 [13,16,17]
XEINT26/KP_ROW2 [13,16,17]
XEINT27/KP_ROW3 [7,13,16,17]
EXT_nRESET [6,19]
XEINT28/KP_ROW4 [6,13,16]
XEINT29/KP_ROW5 [13,16]
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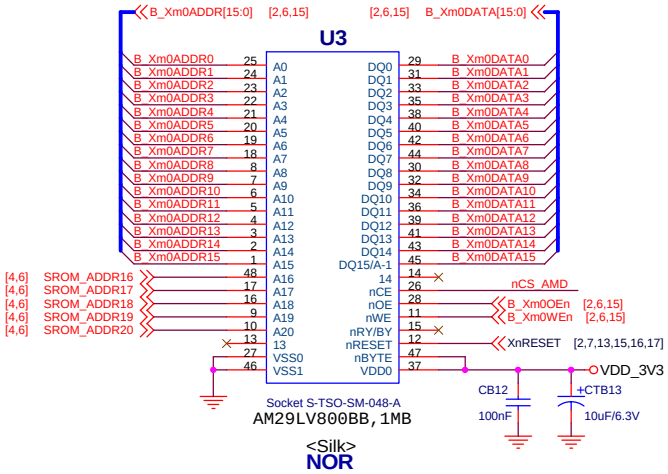
XEINT31/KP_ROW7 [13,16,18]
SPI_CLK1 [16,17]
SPI_CSn1 [16,17]
SPI_MISO1 [16,17]
SPI_MOSI1 [16,17]
SPI_CLK0 [16]
SPI_CSn0 [16]
SPI_MISO0 [16]
SPI_MOSI0 [16]
Xi2cSDA0 [6,7,10,11,16,17]
Xi2cSCL0 [6,7,10,11,16,17]
Xi2cSDA1 [11]
Xi2cSCL1 [11]
XmsmREn/KP_ROW11/CF_IORN/MHL_IDCK [4]
XmsmIRQn/KP_ROW12/CF_IOWN/MHL_VSYNC [4]
XmsmDATA0/KP_COL1/CF_DATA0/MHL_D7 [4]
XmsmDATA1/KP_COL2/CF_DATA1/MHL_D8 [4]
XmsmDATA2/KP_COL3/CF_DATA3/MHL_D9 [4]
XmsmDATA3/KP_COL4/CF_DATA3/MHL_D10 [4]
XmsmDATA4/KP_COL5/CF_DATA4/MHL_D11 [4]
XmsmDATA5/KP_COL6/CF_DATA5/MHL_D12 [4]
XmsmDATA6/KP_COL7/CF_DATA6/MHL_D13 [4]
XmsmDATA7/KP_ROW0/CF_DATA7/MHL_D14 [4]
XmsmDATA8/KP_ROW1/CF_DATA8/MHL_D15 [4]
XmsmDATA9/KP_ROW2/CF_DATA9/MHL_D16 [4]
XmsmDATA10/KP_ROW3/CF_DATA10/MHL_D17 [4]
XmsmDATA11/KP_ROW4/CF_DATA11/MHL_D18 [4]
XmsmDATA12/KP_ROW5/CF_DATA12/MHL_D19 [4]
XmsmDATA13/KP_ROW6/CF_DATA13/MHL_D20 [4]
XmsmDATA14/KP_ROW7/CF_DATA14/MHL_D21 [4]
XmsmDATA15/KP_ROW8/CF_DATA15/MHL_D22 [4]
XpcmSCLK0/SPDIF_OUT0/Xi2sSCLK2 [6,8]
XpcmEXTCLK0/SPDIF_EXTCLK/Xi2sCDCLK2 [6,8]
XpcmFSYNC0/LCD_FRM/Xi2sLRCK2 [8]
XpcmSIN0/Xi2sSDI2 [8]
XpcmSOUT0/Xi2sSDO2 [8]
XpwmTOUT0 [5,18]
XpwmTOUT1 [6,14,16,18]
XpwmTOUT2 [6,14,16,18]
XpwmTOUT3/PWM_MIE [18]
Xm0WAITn [3,6]
Xm0FRnB0/ONDXL_INT0 [3]
Xm0FRnB1/ONDXL_INT1 [3]
Xm0FRnB2 [3]
Xm0FRnB3 [3]
B_Xm0OEn [3,6,15]
B_Xm0WEn [3,6,15]
B_Xm0BE0 [3]
B_Xm0BE1 [3]
B_Xm0FCLE/ONDAVD [3,6]
B_Xm0FALE/ONDSMCLK [3]
B_Xm0FWEn/ONDRPn [3]
B_Xm0FREn [3]
B_Xm0ADDR[15:0] [3,6,15]
B_Xm0DATA[15:0] [3,6,15]
XmsmCSn/KP_ROW9/CF_CSn0/MHL_D23 [4]
XmsmWEn/KP_ROW10/CF_CSn1/MHL_HSYNC [4]
XmsmADDR0/CAM_B_D0/CF_ADDR0/MIPI_BYTE_CLK [4,7]
XmsmADDR1/CAM_B_D1/CF_ADDR1/MIPI_ESC_CLK [4,7]
XmsmADDR2/CAM_B_D2/CF_ADDR2/TS_CLK [4,7]
XmsmADDR3/CAM_B_D3/CF_IORDY/TS_SYNC [4,7]
XmsmADDR4/CAM_B_D4/CF_INTRQ/TS_VAL [4,7]
XmsmADDR5/CAM_B_D5/CF_DMARQ/TS_DATA [4,7]
XmsmADDR6/CAM_B_D6/CF_DRESETN/TS_ERROR [4,7]
XmsmADDR7/CAM_B_D7/CF_DMACKN/MHL_D0 [4,7]
XmsmADDR8/CAM_B_PCLK/SROM_ADDR16/MHL_D1 [4,7]
XmsmADDR9/CAM_B_VSYNC/SROM_ADDR17/MHL_D2 [4,7]
XmsmADDR10/CAM_B_HREF/SROM_ADDR18/MHL_D3 [4,7]
XmsmADDR11/CAM_B_FIELD/SROM_ADDR19/MHL_D4 [4,7]
XmsmADDR12/CAM_B_CLKOUT/SROM_ADDR20/MHL_D5 [4,7]
XmsmADDR13/KP_COL0/SROM_ADDR21/MHL_D6 [4]
XmsmADVN/KP_ROW13/SROM_ADDR22/MHL_DE [4]
XCLKOUT [10]
PWROn_BOARD [7,16,17]
Xm0DATA_RDn
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
DC5V
CTB1
CTB2
CTB3
CTB4
CTB5
CTB6
CTB7
CTB8
CTB9
CB1
CB2
CB3
CB4
CB5
CB6
CB7
CB8
CB9
CB10
100nF
10uF/6.3V
10uF/10V
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)
Size
A3
Document Number
B2B Connector(Base)
Rev
0.1
Date:
Thursday, October 01, 2009
Sheet
2
of
19

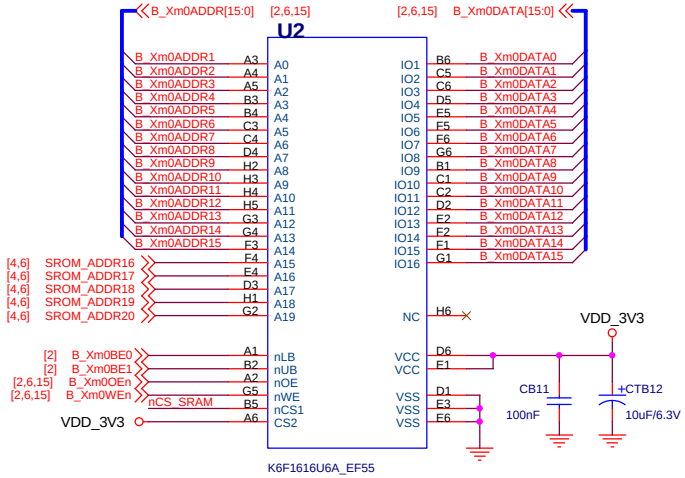
AMD NOR-Flash Memory(SOCKET)



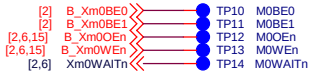
<Silk>
NOR

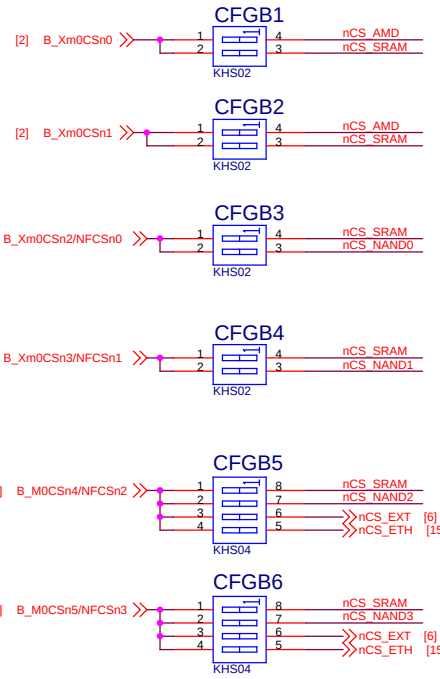
ADDR for SRAM is using byte base addressing

SRAM Memory

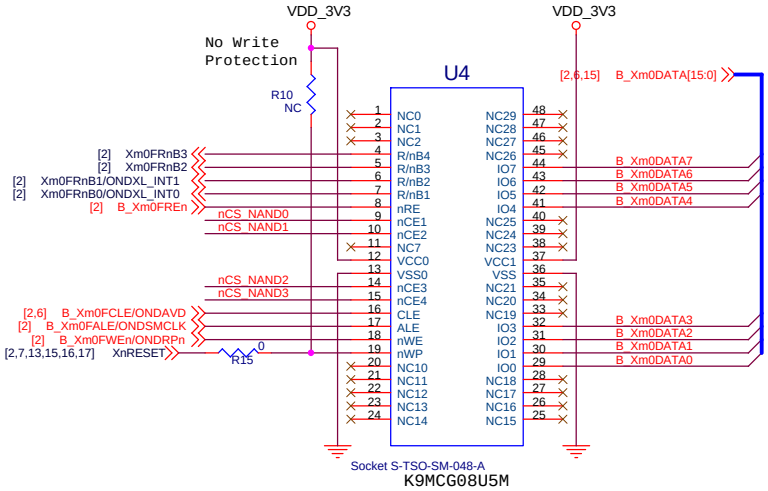


<Silk>
SRAM

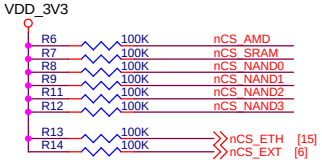




Samsung NAND-Flash memory(SOCKET)



<Silk>
NAND



<Silk>

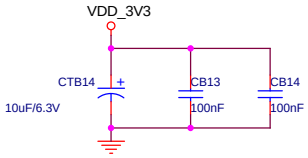
CFGB1:nCS0	CFGB2:nCS1
[2]	SRAM
[1]	NOR

CFGB3:nCS2	
[2]	NAND CS0
[1]	SRAM

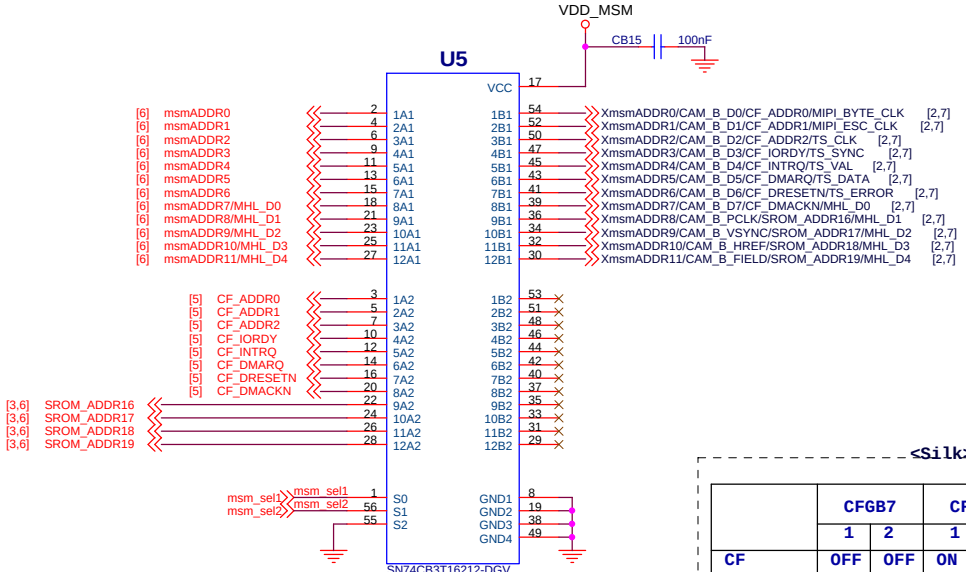
CFGB4:nCS3	
[2]	NAND CS1
[1]	SRAM

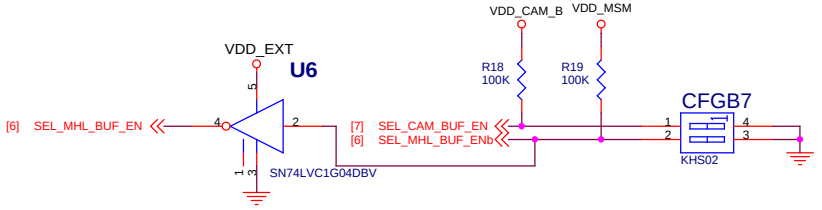
CFGB5:nCS4	
[4]	Ethernet
[3]	External
[2]	NAND CS2
[1]	SRAM

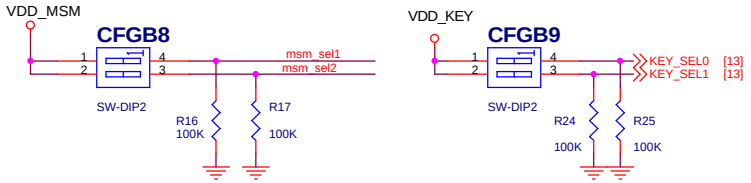
CFGB6:nCS5	
[4]	Ethernet
[3]	External
[2]	NAND CS3
[1]	SRAM



SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size: A3	Document Number: NOR/NAND/SRAM/xD Card/Chip Selection	Rev: 0.1
Date: Thursday, October 01, 2009	Sheet 3 of 19	





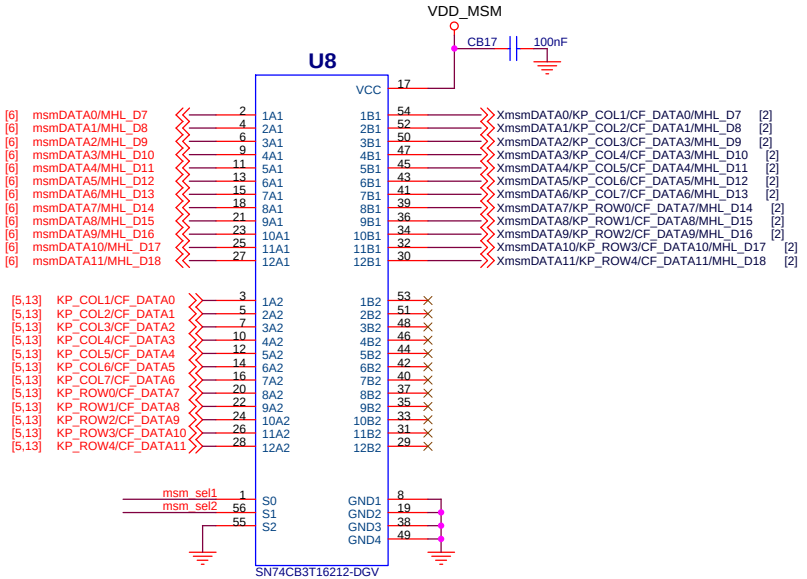


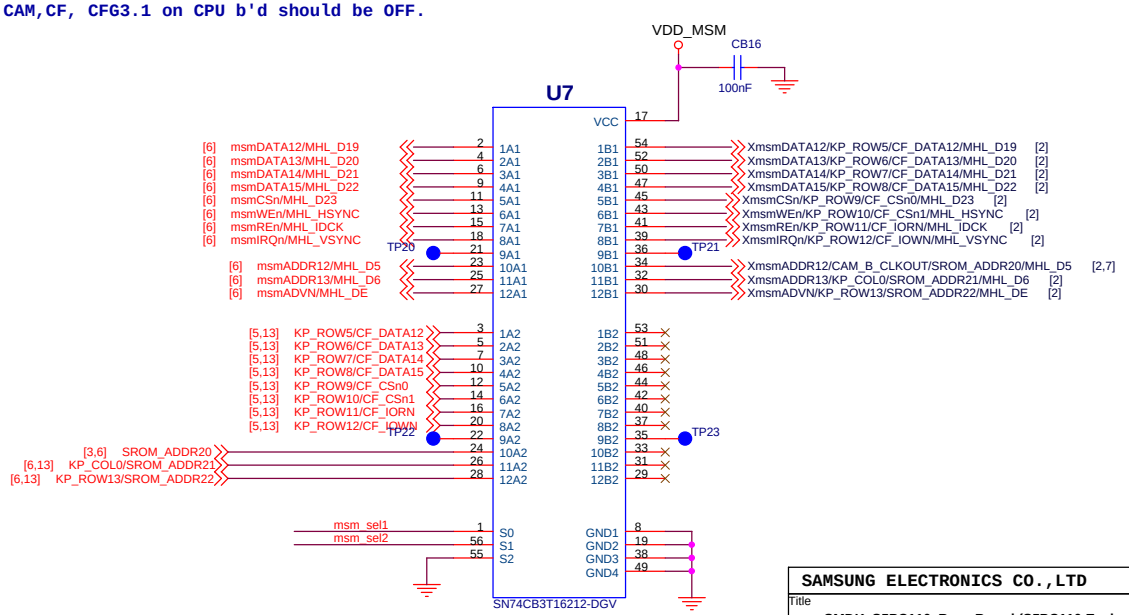
	CFGB7		CFGB8		CFGB9	
	1	2	1	2	1	2
CF	OFF	OFF	ON	ON	OFF	OFF
SROM	OFF	OFF	ON	ON	OFF	OFF
MHL	OFF	ON	ON	OFF	OFF	OFF
MSM	OFF	OFF	ON	OFF	OFF	OFF
CAM	ON	OFF	OFF	OFF	OFF	OFF
KEY(MSM)	OFF	OFF	ON	ON	ON	ON
KEY(INT)					ON	OFF

S2	S1	S0	
L	L	L	Disconnect
L	L	H	A1 = B1
L	H	H	A2 = B1

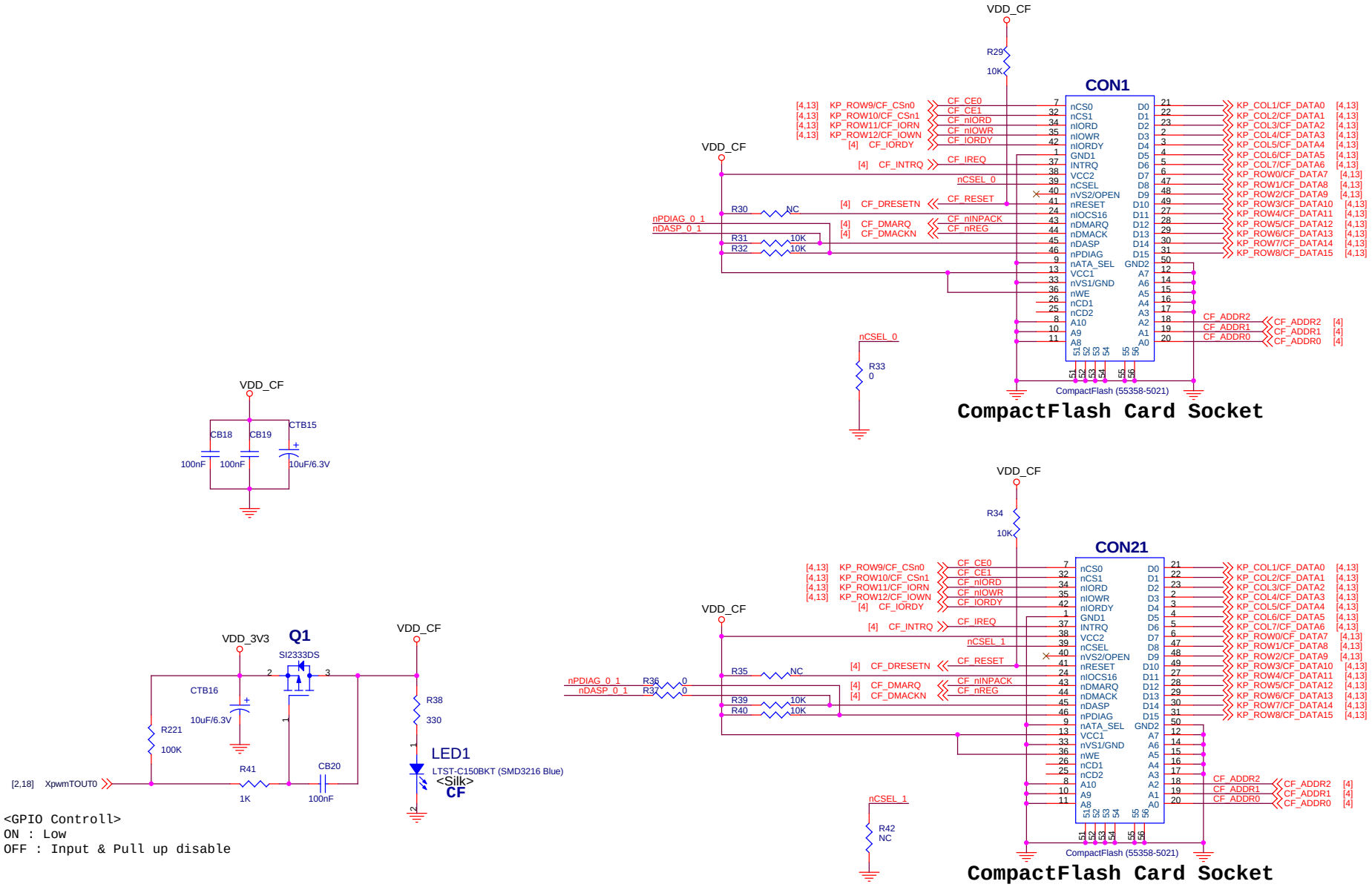
*KEY(MSM) case: Remove CF card & don't access SROM.

*To use MSM,CAM,CF, CFG3.1 on CPU b'd should be OFF.

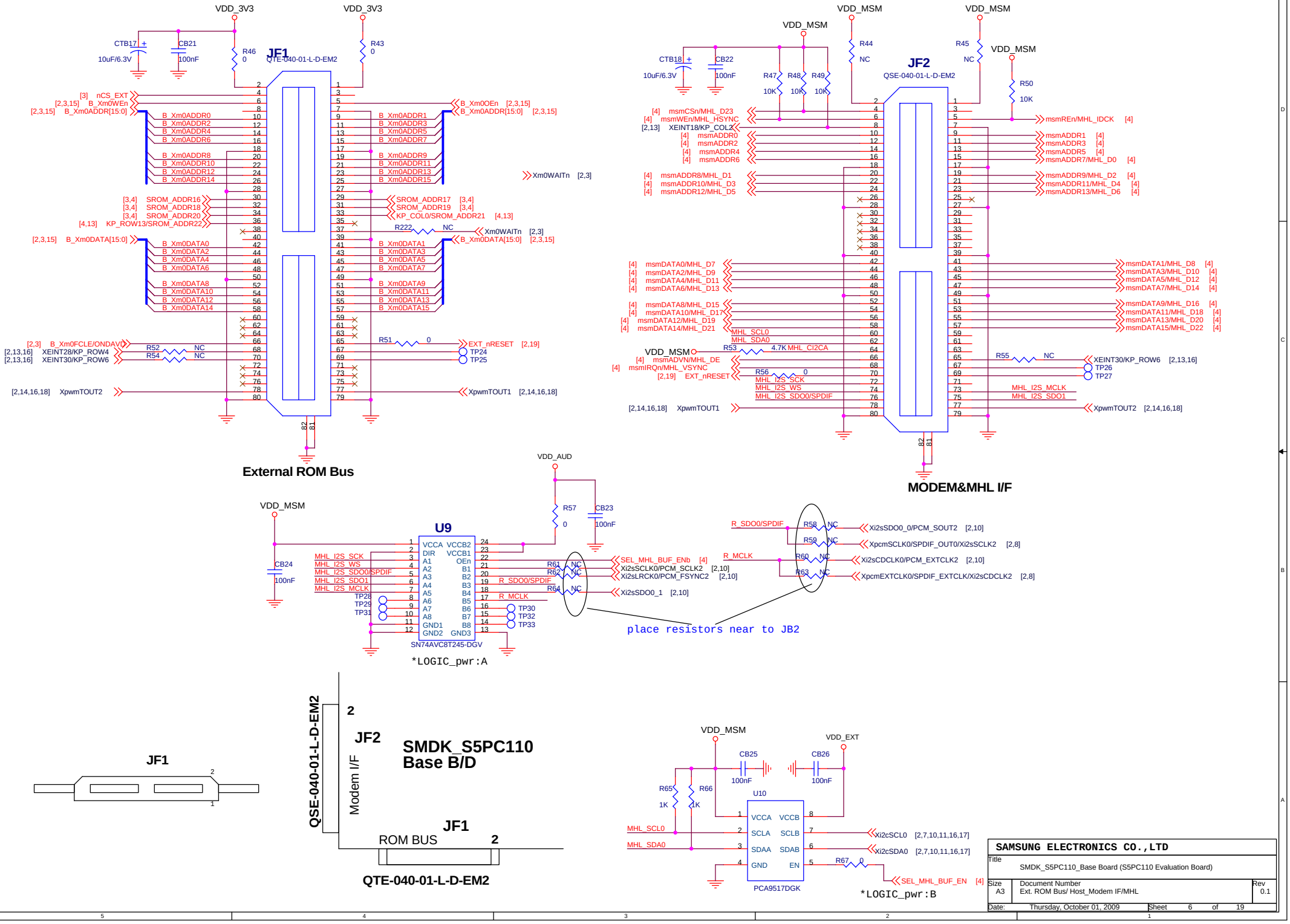




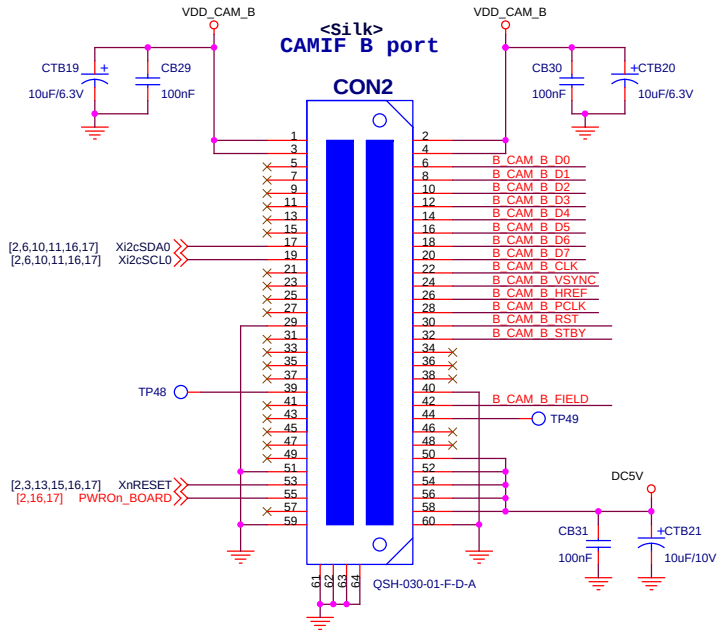
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size: A3	Document Number: CF,modem,key switching	Rev: 0.1
Date: Thursday, October 01, 2009	Sheet 4 of 19	

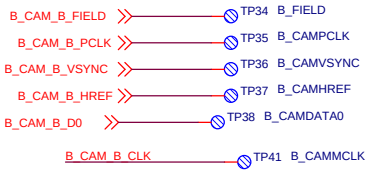


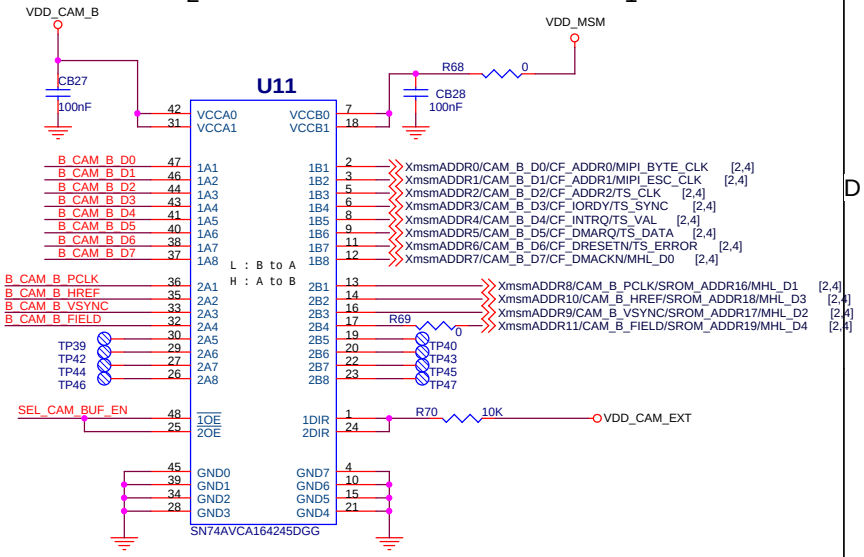
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size: A3	Document Number: Compact Flash Card Socket	Rev: 0.1
Date: Thursday, October 01, 2009	Sheet 5 of 19	

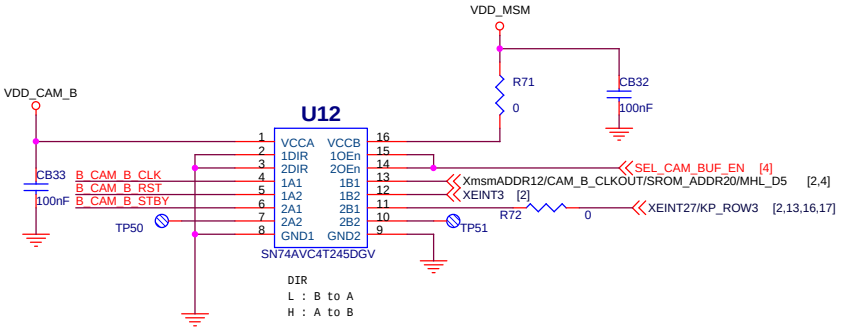

External ROM Bus
MODEM&MHL I/F
JF1
QTE-040-01-L-D-EM2
JF2
QSE-040-01-L-D-EM2
SMDK_S5PC110
Base B/D
Modem I/F
ROM BUS
U9
SN74AVC8T245-DGV
U10
PCA9517DGK
*LOGIC_pwr:A
*LOGIC_pwr:B
place resistors near to JB2
SAMSUNG ELECTRONICS CO.,LTD
SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)
Ext. ROM Bus/ Host_Modem IF/MHL
Thursday, October 01, 2009
Sheet 6 of 19

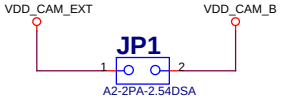
CAM B

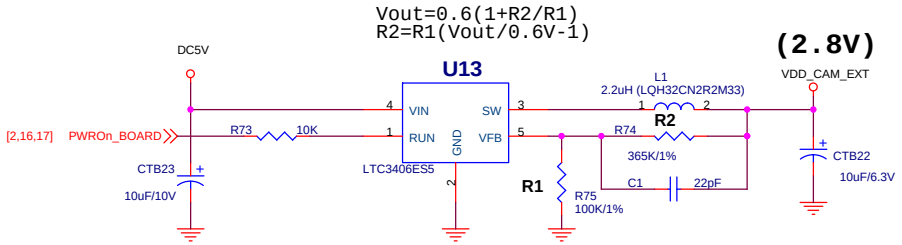




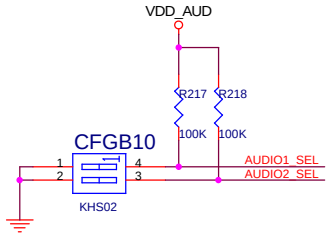








SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size: A3	Document Number: Camera I/F B Port	Rev: 0.1
Date: Thursday, October 01, 2009	Sheet 7 of 19	



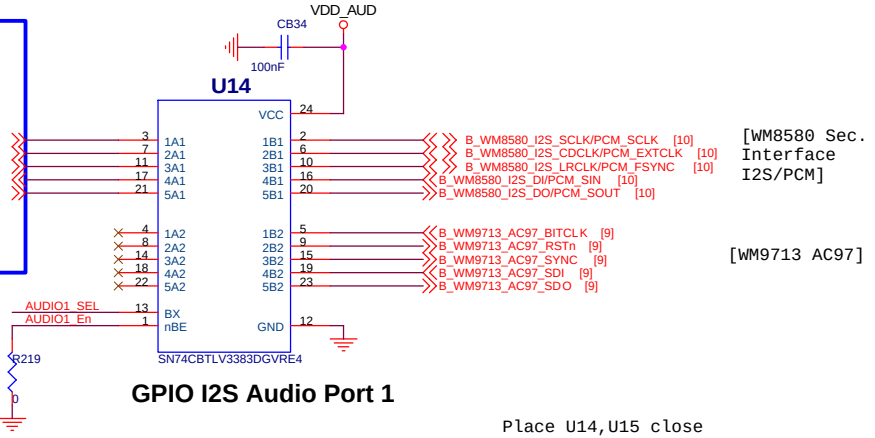
<Silk>

CFGB10	[1]	[2]
Off	Audio1: WM9713 AC97	Audio2: SPDIF OUt
On	Audio1: WM8580 IIS/PCM	Audio2: WM8580 IIS/PCM

SCLK, LRCLK, SDO should have same routing length!!!
CDCLK(max 24MHz) should be guarded by ground!!!

[2] Xi2sSCLK1/PCM_SCLK1/AC97_BITCLK
[2] Xi2sCDCLK1/PCM_EXTCLK1/AC97_RESETn
[2] Xi2sLRCK1/PCM_FSYNC1/AC97_SYNC
[2] Xi2sSDI1/PCM_SIN1/AC97_SDI
[2] Xi2sSDO1/PCM_SOUT1/AC97_SDO

[I2S1/PCM1/AC97]



[WM8580 Sec. Interface I2S/PCM]

[WM9713 AC97]

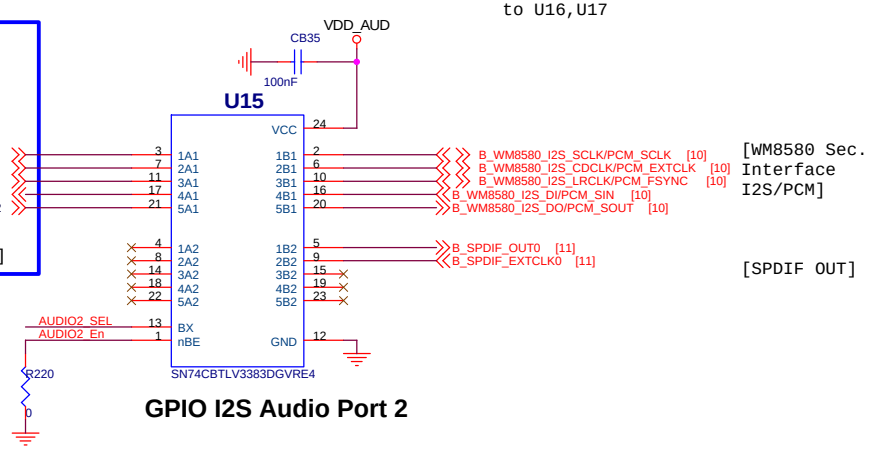
GPIO I2S Audio Port 1

Place U14,U15 close to U16,U17

SCLK, LRCLK, SDO should have same routing length!!!
CDCLK(max 24MHz) should be guarded by ground!!!

[2,6] XpcmSCLK0/SPDIF_OUT0/Xi2sSCLK2
[2,6] XpcmEXTCLK0/SPDIF_EXTCLK/Xi2sCDCLK2
[2] XpcmFSYNC0/LCD_FRM/Xi2sLRCK2
[2] XpcmSIN0/Xi2sSDI2
[2] XpcmSOUT0/Xi2sSDO2

[I2S2/PCM0/SPDIF]



[WM8580 Sec. Interface I2S/PCM]

[SPDIF OUT]

GPIO I2S Audio Port 2

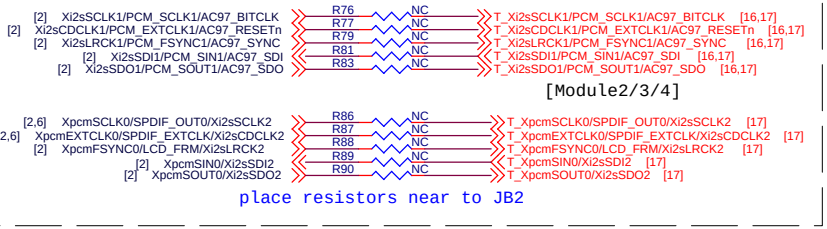
SCLK, LRCLK, SDO should have same routing length!!!
CDCLK(max 24MHz) should be guarded by ground!!!

[I2S0/PCM2]

GPIO I2S Audio Port 0

[WM8580 Pri I2S/PCM]

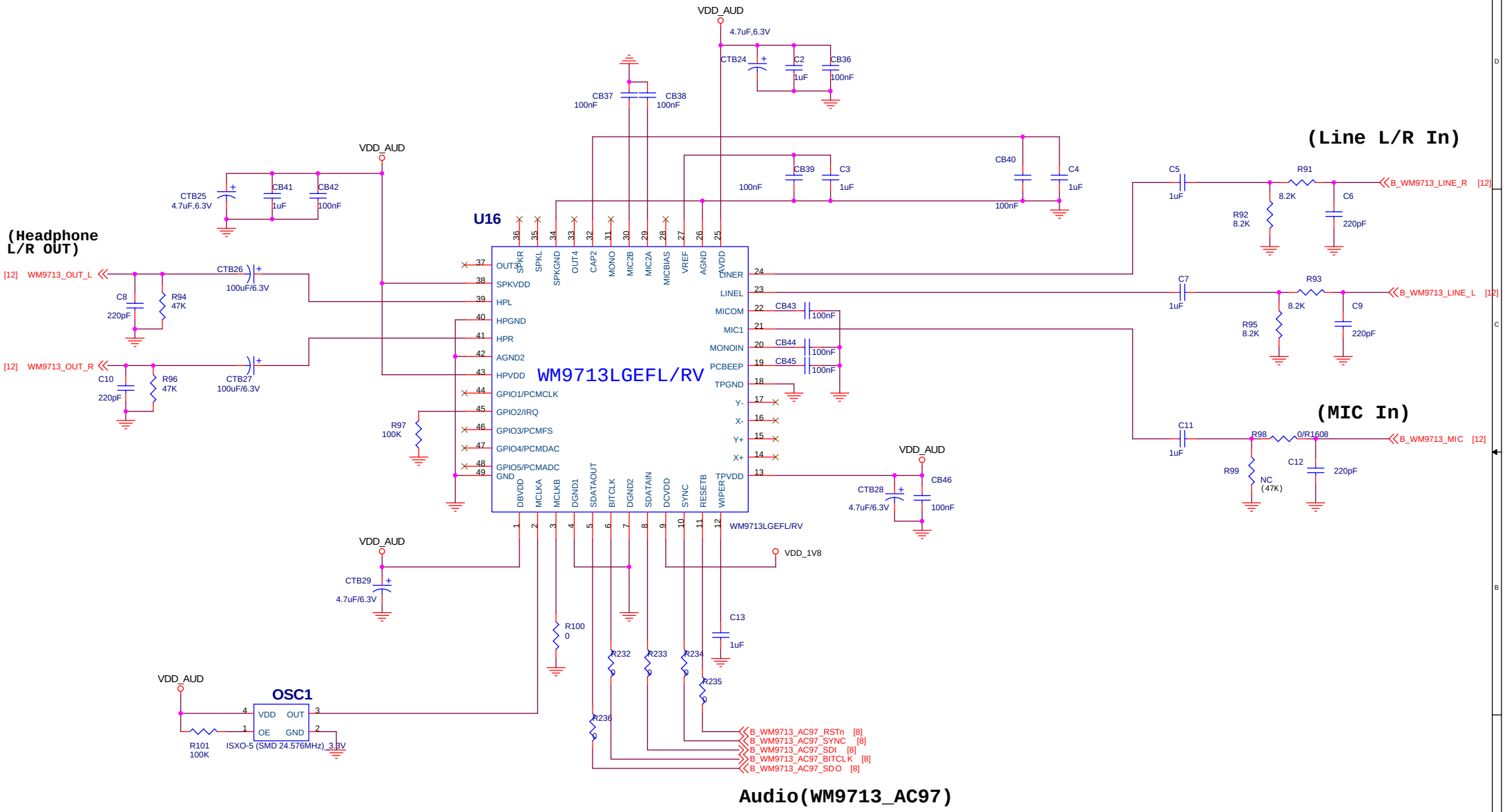
[For isolate purpose only] - Since these are shared with other module



[Module2/3/4]

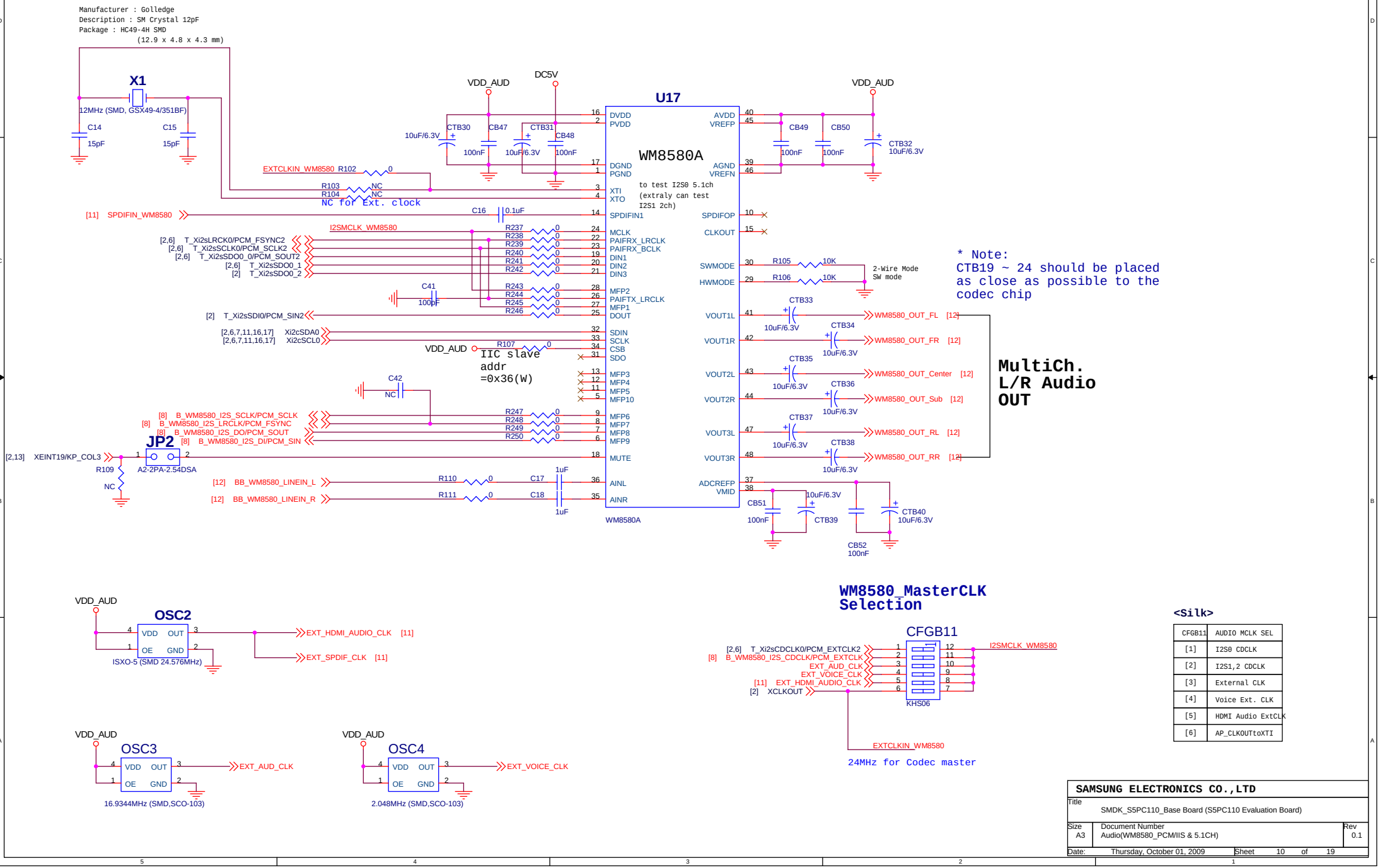
place resistors near to JB2

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size: A3	Document Number: Audio Switch	Rev: 0.1
Date: Thursday, October 01, 2009	Sheet 8 of 19	



SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size: A3	Document Number: Audio(WM9713_AC97)	Rev: 0.1
Date: Thursday, October 01, 2009	Sheet 9 of 19	

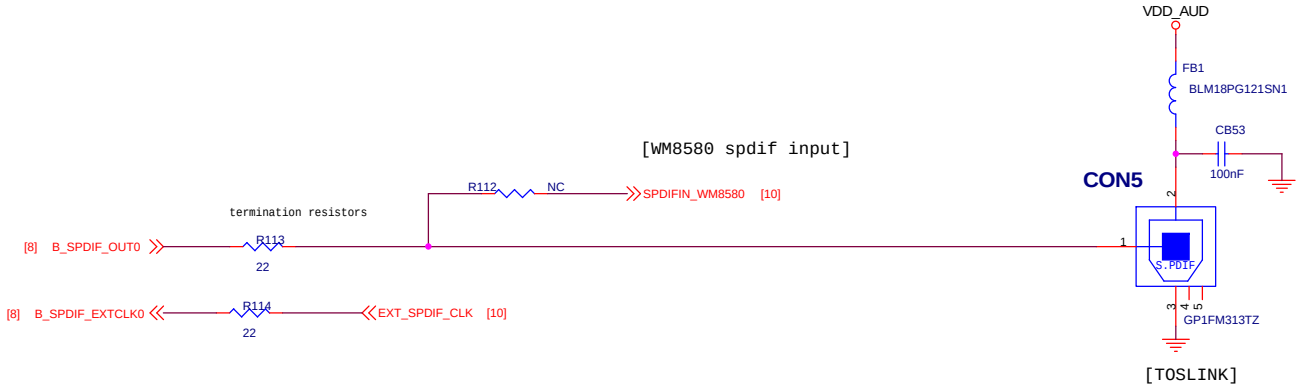
Audio(WM8580_PCM/IIS & 5.1CH)



<Silk>

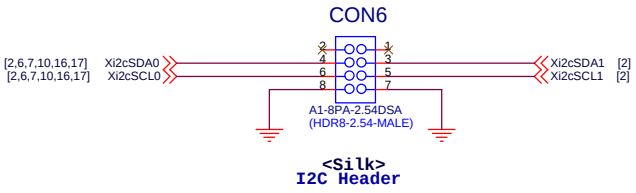
CFGB11	AUDIO MCLK SEL
[1]	I2S0 CDCLK
[2]	I2S1,2 CDCLK
[3]	External CLK
[4]	Voice Ext. CLK
[5]	HDMI Audio ExtCLK
[6]	AP_CLKOUTtoXTI

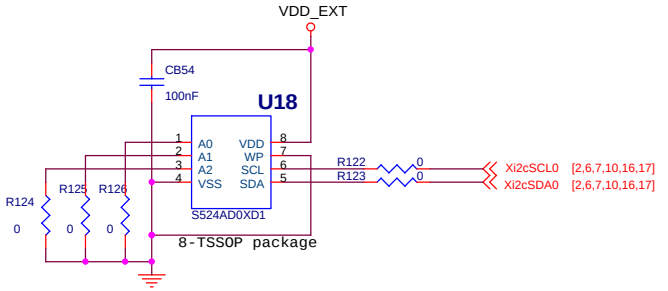
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size: A3	Document Number: Audio(WM8580_PCM/IIS & 5.1CH)	Rev: 0.1
Date: Thursday, October 01, 2009	Sheet 10 of 19	



S/PDIF Audio Out

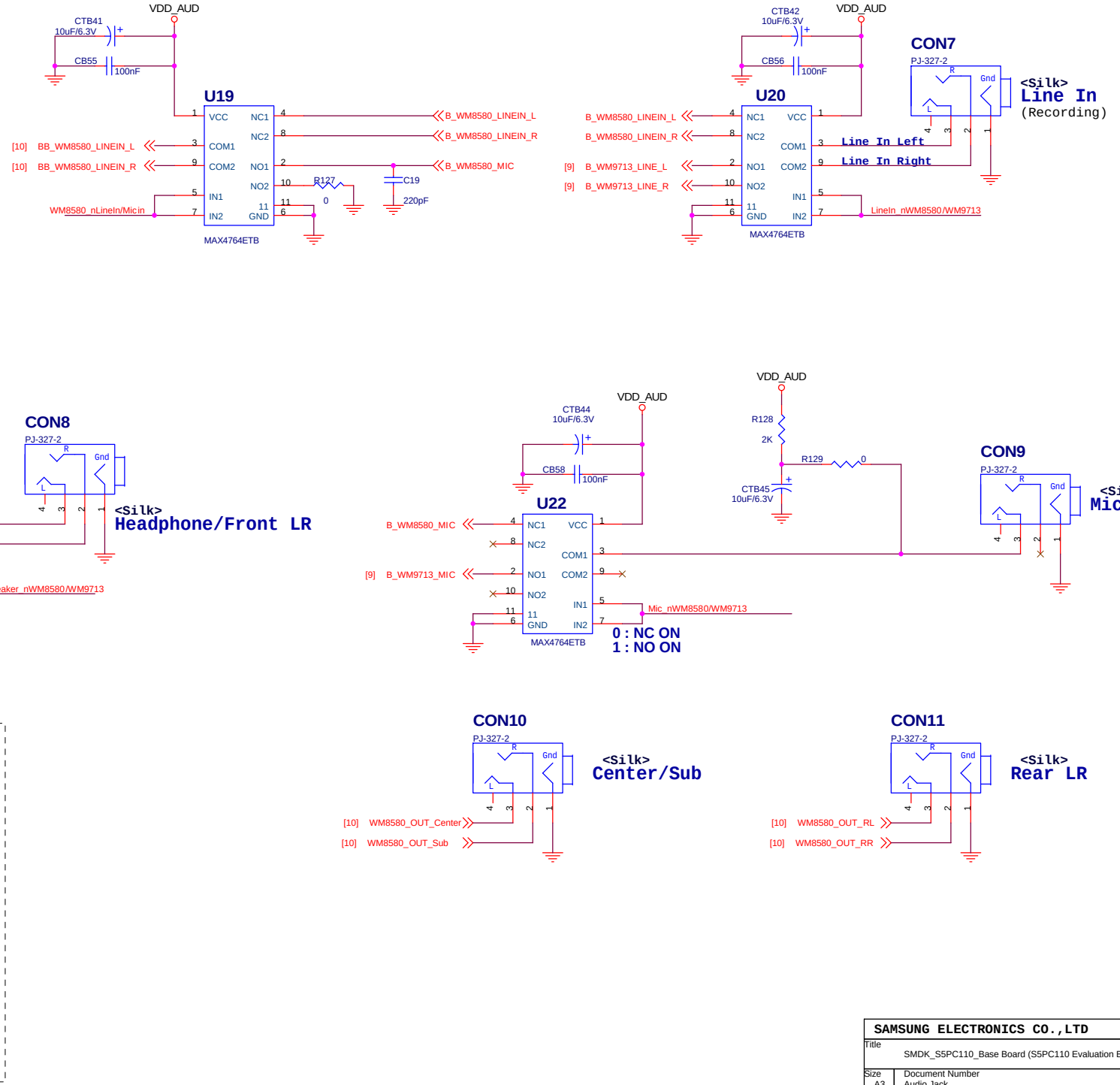
For Multi_Master I2C



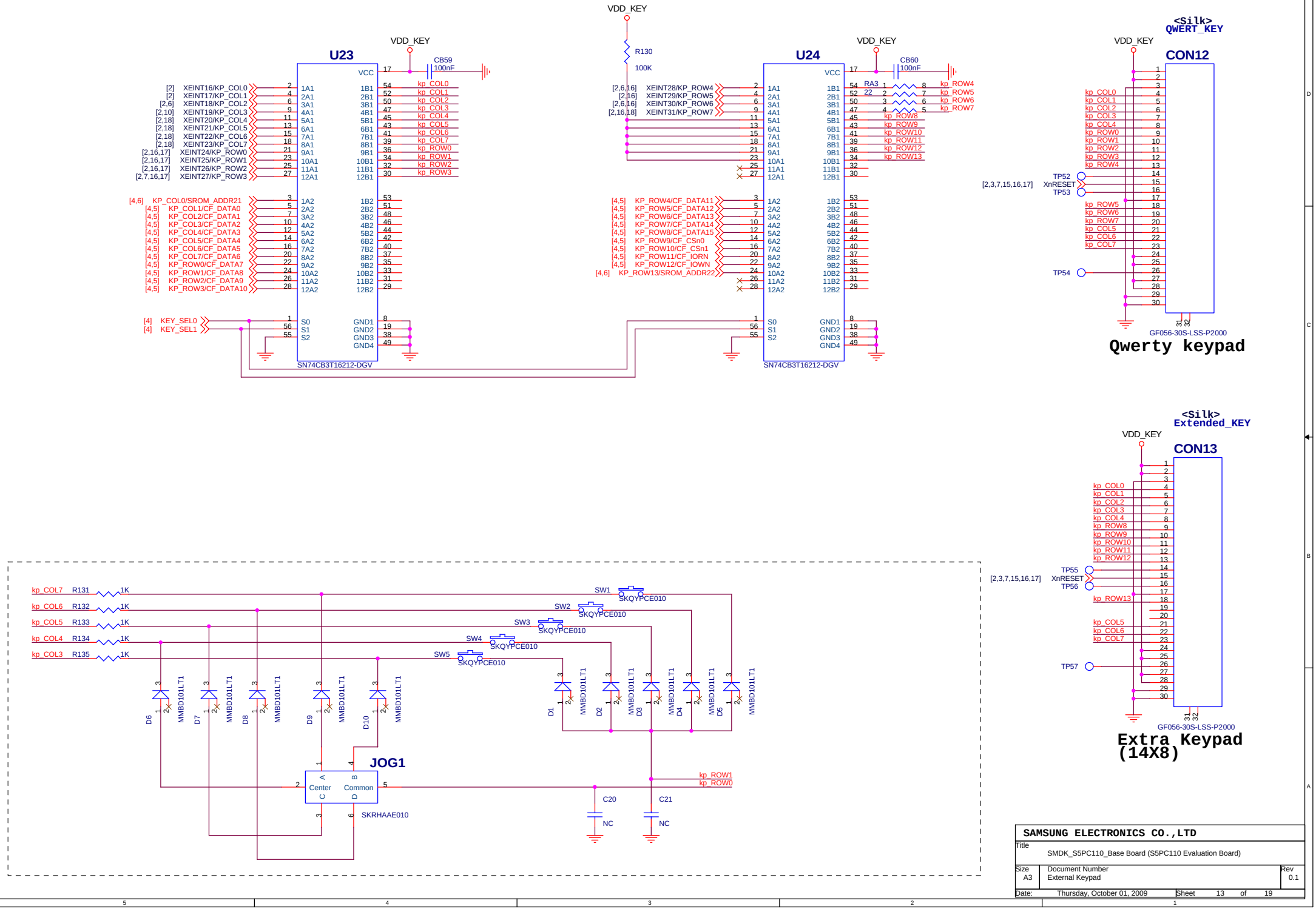


IIC E2PROM

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size: A3	Document Number: SPDIF Out / IIC EEPROM	Rev: 0.1
Date: Thursday, October 01, 2009	Sheet 11 of 19	



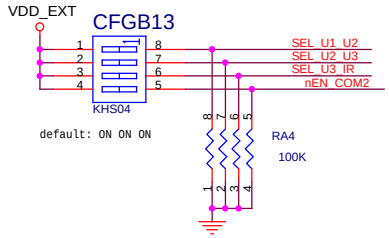
SAMSUNG ELECTRONICS CO.,LTD	
Title: SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)	
Size: A3	Document Number: Audio Jack
Rev: 0.1	
Date: Thursday, October 01, 2009	Sheet 12 of 19

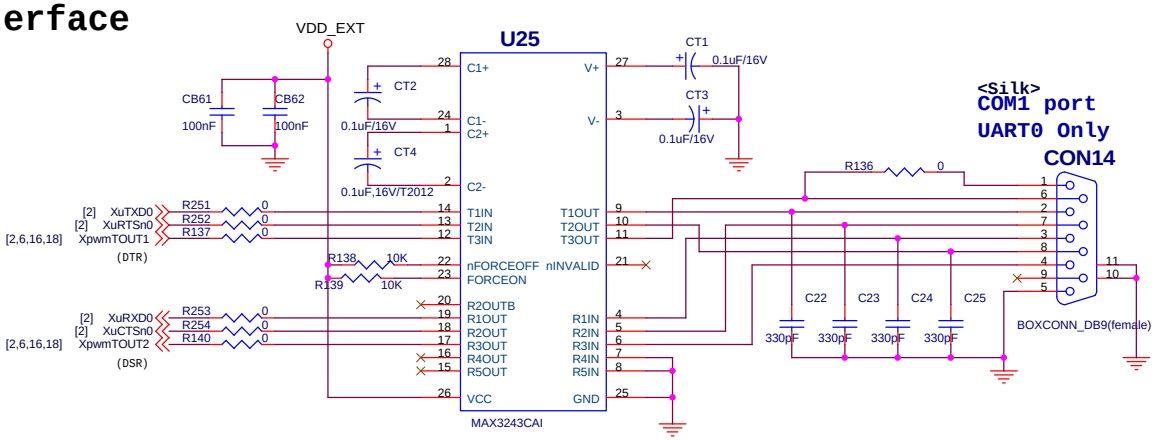

U23
U24
VDD_KEY
CB59
CB60
100nF
R130
100K
SN74CB3T16212-DGV
KEY_SEL0
KEY_SEL1
RA3
22
<Silk>
QWERT_KEY
CON12
TP52
TP53
TP54
XnRESET
GF056-30S-LSS-P2000
Qwerty keypad
<Silk>
Extended_KEY
CON13
TP55
TP56
TP57
Extra Keypad
(14X8)
R131
R132
R133
R134
R135
1K
SW1
SW2
SW3
SW4
SW5
SKQYPCE010
MMBD101LT1
JOG1
Center
Common
SKRHAAE010
C20
C21
NC
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)
Size
A3
Document Number
External Keypad
Rev
0.1
Date:
Thursday, October 01, 2009
Sheet
13
of
19

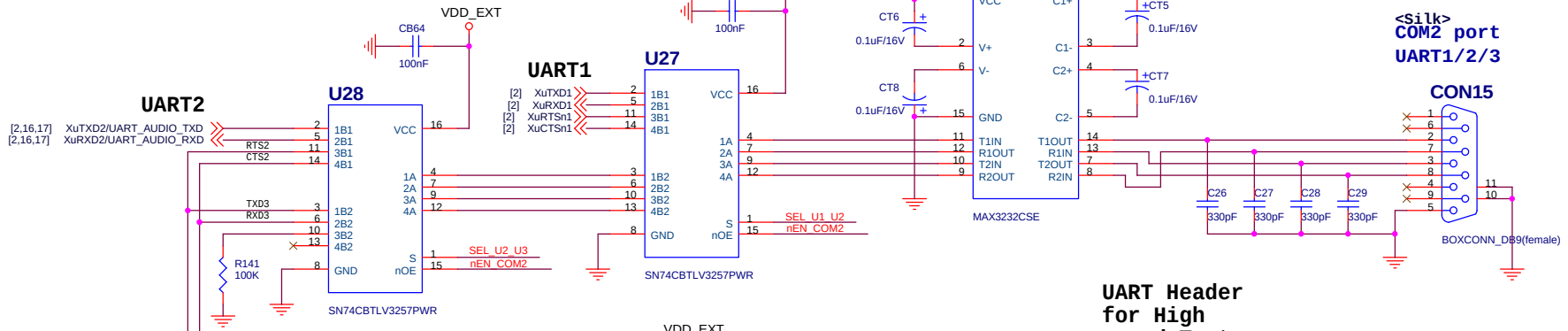
UART / IrDA Interface

<Silk>

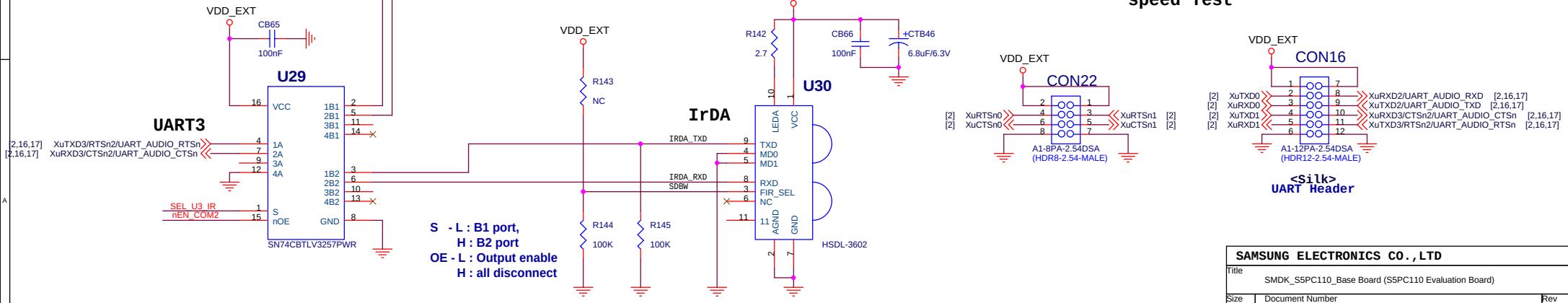
CFGB13:COM2	PIN1	PIN2	PIN3	PIN4
UART1	OFF	X	X	OFF
UART2	ON	OFF	X	OFF
UART3	ON	ON	OFF	OFF
IrDA(U2)	X	X	ON	OFF



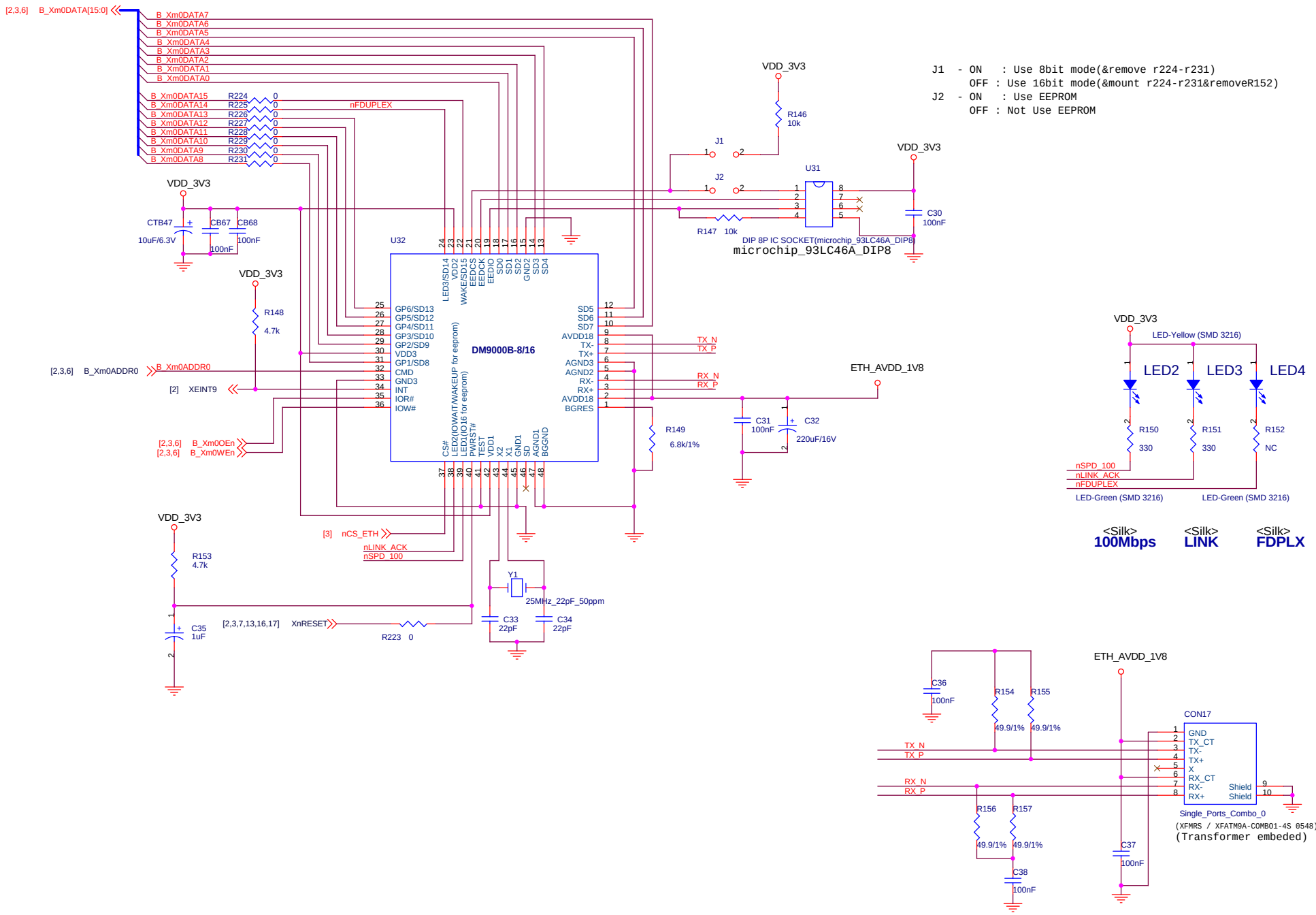




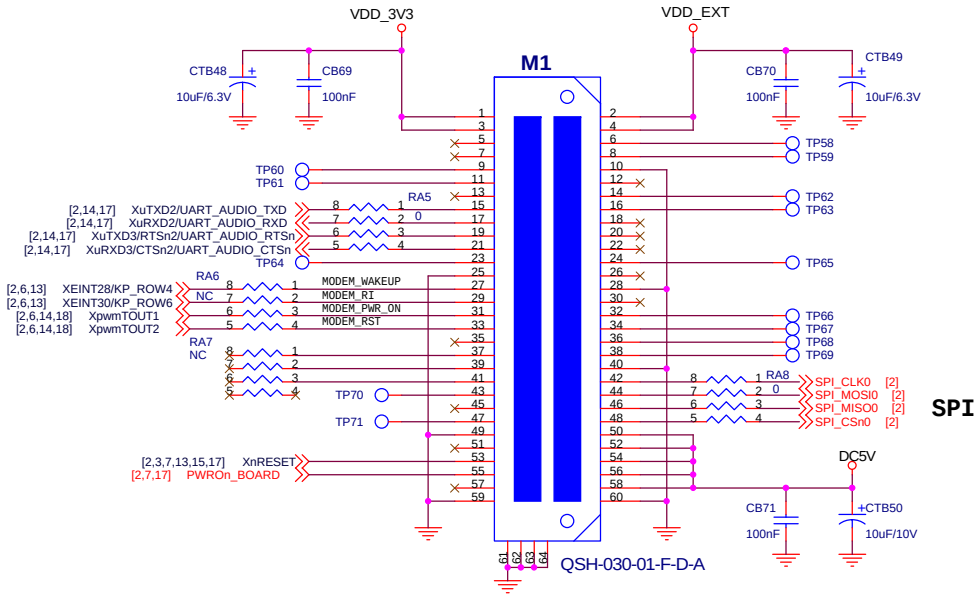
UART Header for High speed Test



SAMSUNG ELECTRONICS CO.,LTD			
Title: SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)			
Size: A3	Document Number: UART/IrDA		Rev: 0.1
Date: Thursday, October 01, 2009	Sheet 14 of 19		

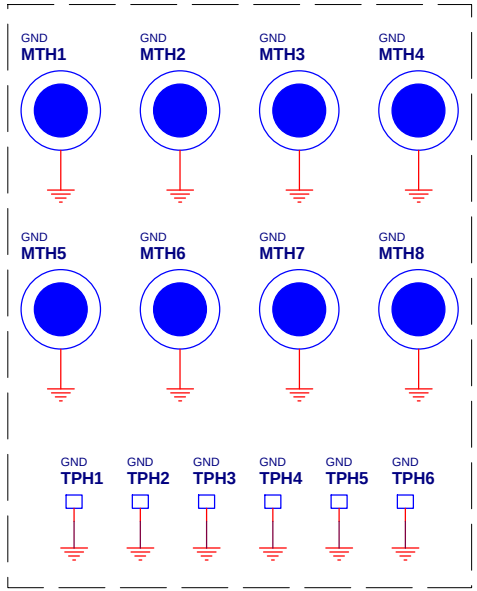


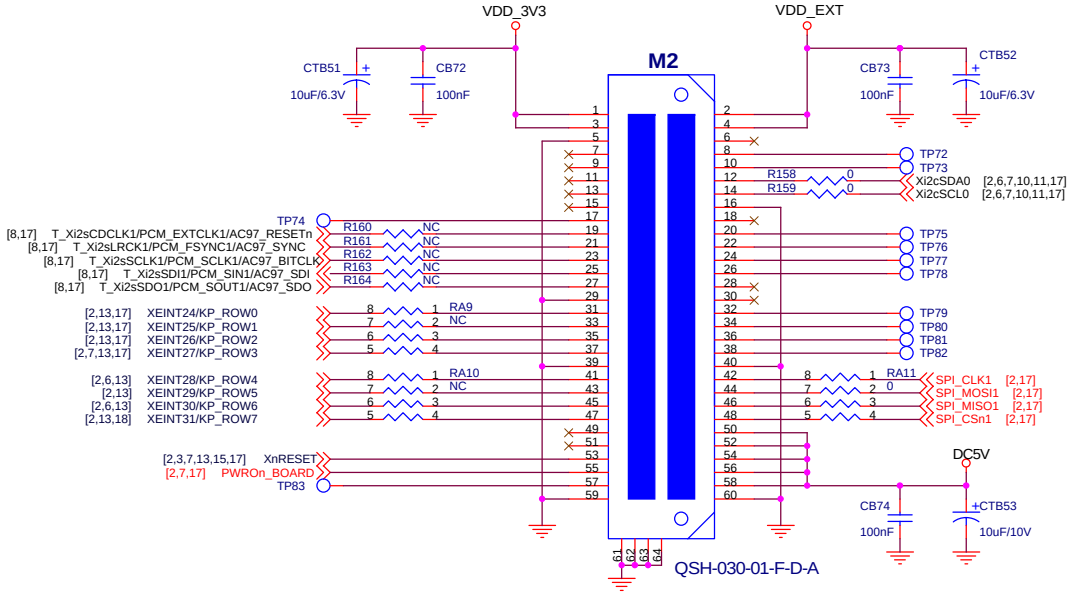
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size: A3	Document Number: Ethernet 100Mbp(DM9000)	Rev: 0.1
Date: Thursday, October 01, 2009	Sheet 15 of 19	



SPI

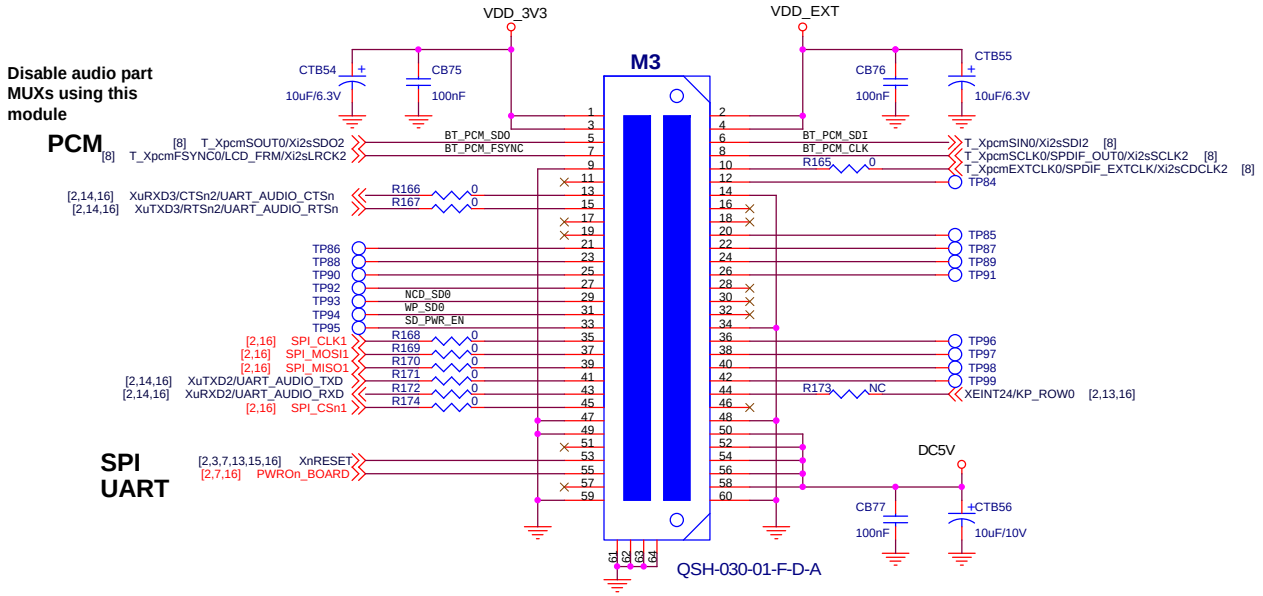
GPS (UART2, SPI0)
MODULE 1





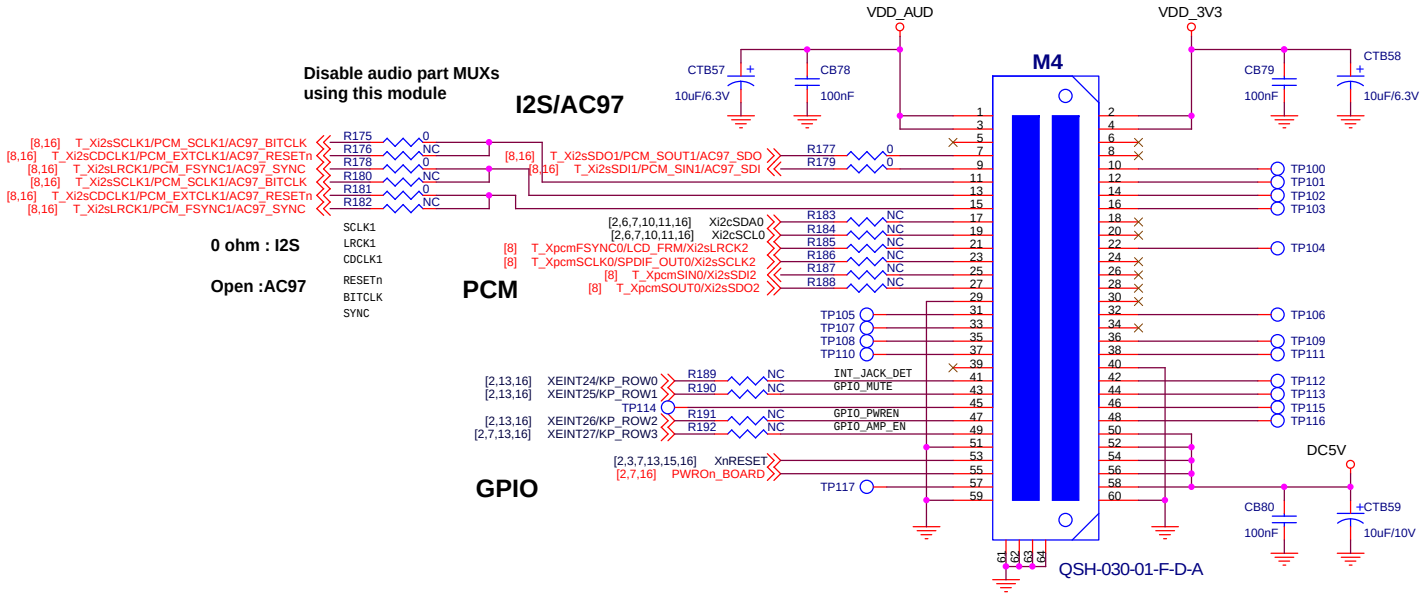
Mobile TV (SPI1, IIC)
HD Radio (SPI1, IIS for Module 4)
MODULE 2

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size: A3	Document Number: Module Connector1&2	Rev: 0.1
Date: Thursday, October 01, 2009	Sheet 16 of 19	



BT (UART2, PCM)

MODULE 3

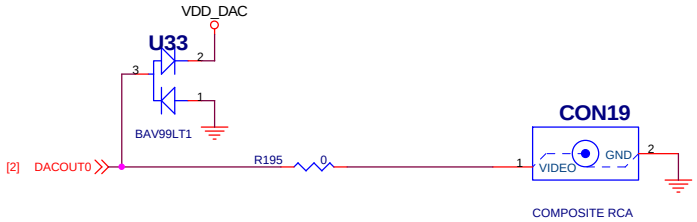


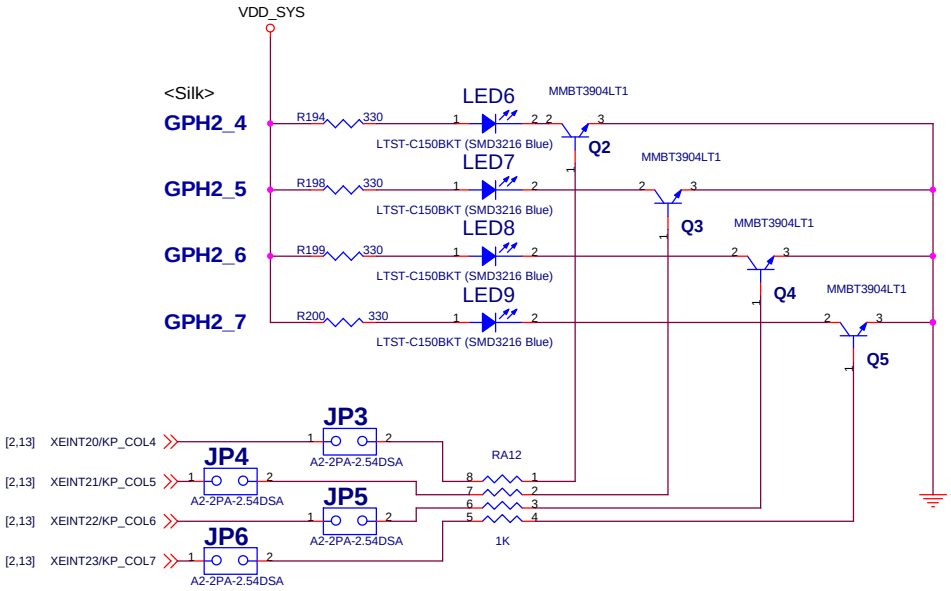
Audio (AC97, IIS, IIC)

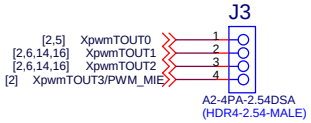
MODULE 4

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size: A3	Document Number: Module Connector3&4	Rev: 0.1
Date: Thursday, October 01, 2009	Sheet 17 of 19	

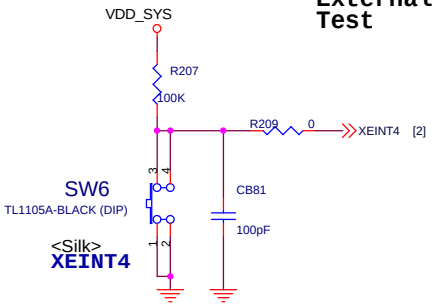
TV Interface

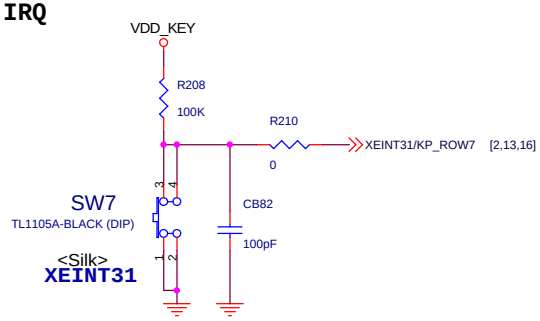


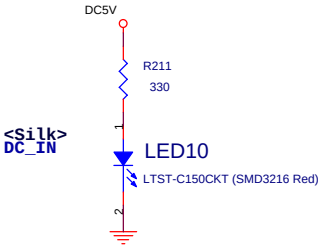




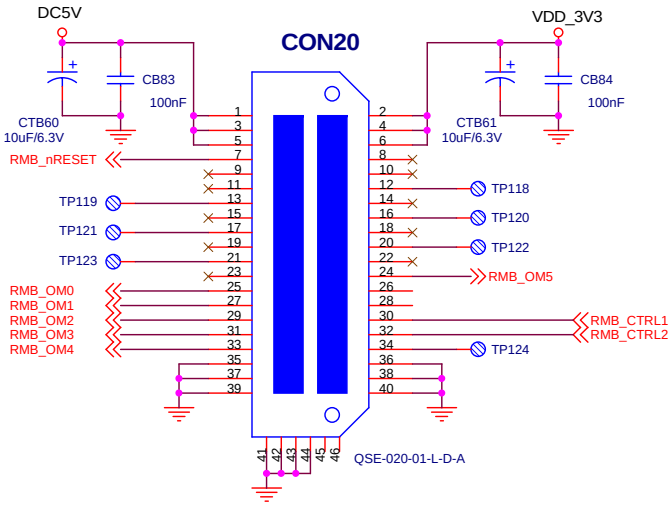
External IRQ Test

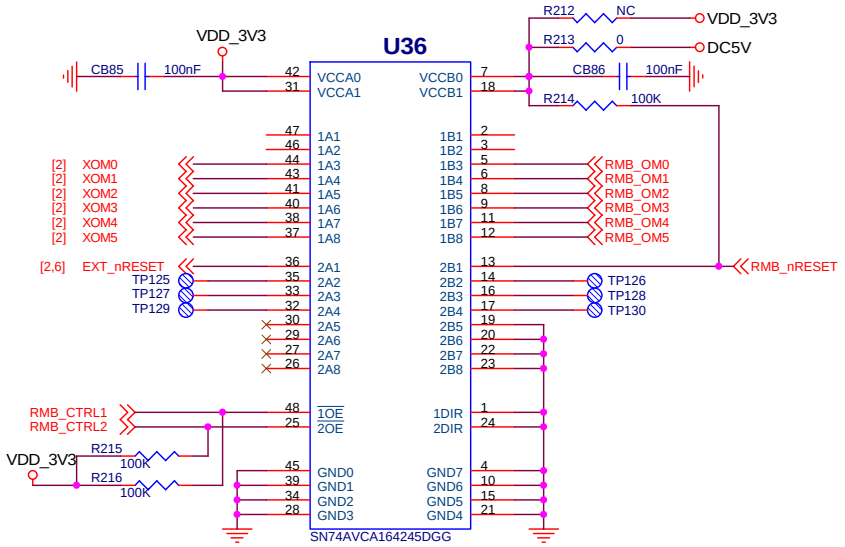






SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size: A3	Document Number: TV Interface/ PWM/ LED/ EINT	Rev: 0.1
Date: Thursday, October 01, 2009	Sheet 18 of 19	





For RMB Board I/F Connector

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size: B	Document Number: RMB b'd IF(for SMDK b'd test)	Rev: 0.1
Date: Thursday, October 01, 2009	Sheet 19 of 19	

SMDK_S5PC110_LCD B'd (S5PC110 Evaluation Board) Schematics

Revision	Date	Description
Rev 0.0	2009. 05.12	Preliminary Version
Rev 0.1		
Rev 0.2		

Table of Contents

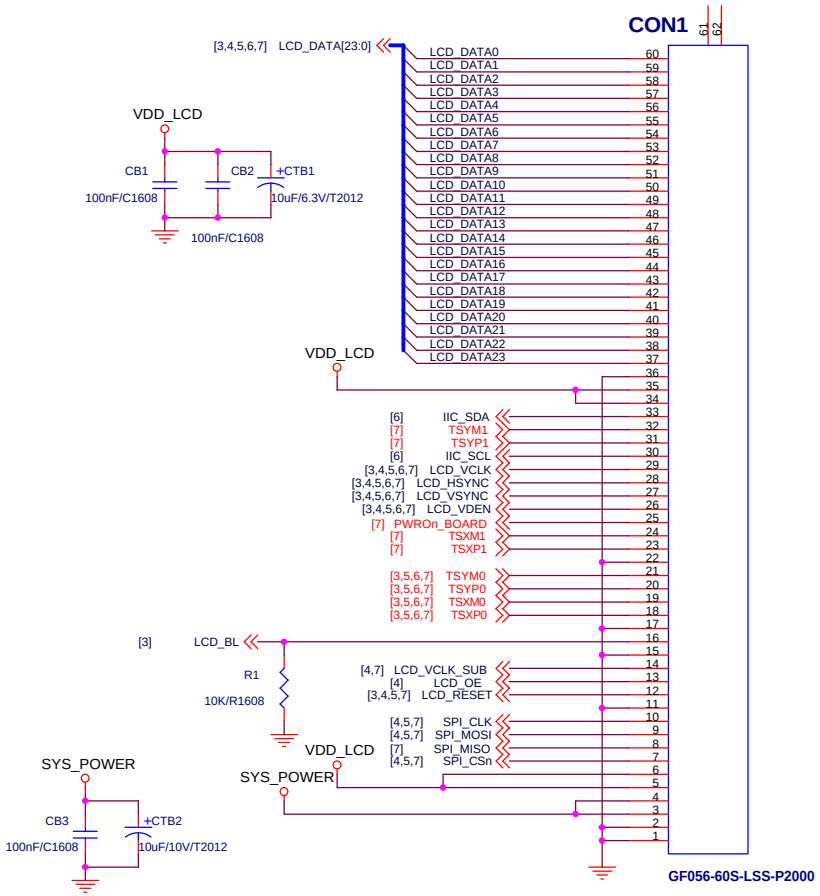
Part Reference

<Component><Number>

U : Component or Regurator IC
C : Capacitor
CB : Capacitor Bypass
CT : Capacitor Tantal
CTB : Capacitor Tantal Bypass
J : Jumper
JB : CPU To Base connector
JP : Jumper Power
R : Resistor
RA : Resistor Array
RP : Resistor Power
VR : Variable Resistor
L : Inductor
FB : Ferrite Bead
OSC : Oscillator
X : X-tal (Crystal)
Q : Transistor or FET
D : Diode
ZD : Zener Diode
LED : LED Diode
SW : SWitch Tact/Push
CON : CONnector
CFG : ConFiGure switch (DIP/Slide)
TP : Test Point (SMD)
TPH : Test Point Hole (Through Hole)
MTH: Mount Through Hole
M (MOD) : MODule Interface connector

Title	SMDK_S5PC110 LCD Board (S5PC110 Evaluation Board)	
Size A3	Document Number Revision History	Rev 0.1
Date: Thursday, October 01, 2009	Sheet 1 of 4	

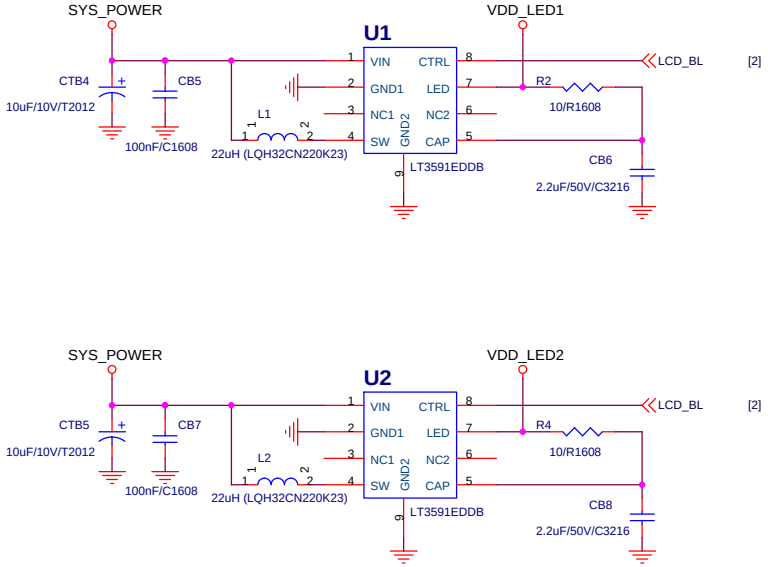
TFT LCD FPC Cable Interface From SMDK

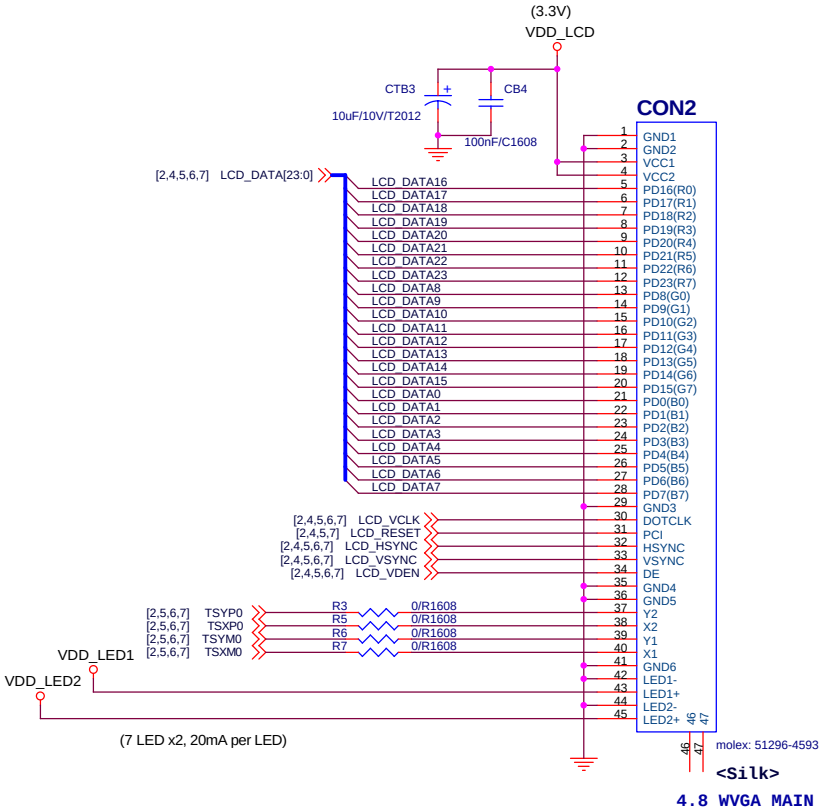


SAMSUNG ELECTRONICS CO.,LTD	
Title	SMDK_S5PC110 LCD Board (S5PC110 Evaluation Board)
Size A3	Document Number Connector to SMDK — Rev 0.1
Date: Thursday, October 01, 2009	Sheet 2 of 4

RGB(24Bit) Parallel Interface

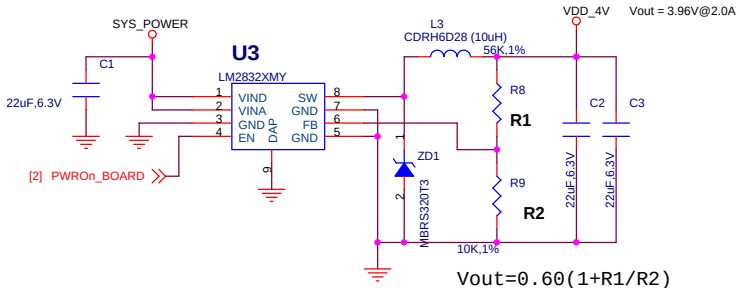
LED drivers (Common)



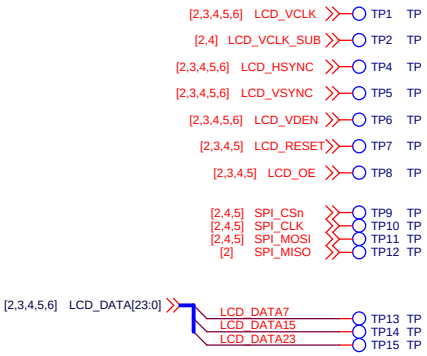


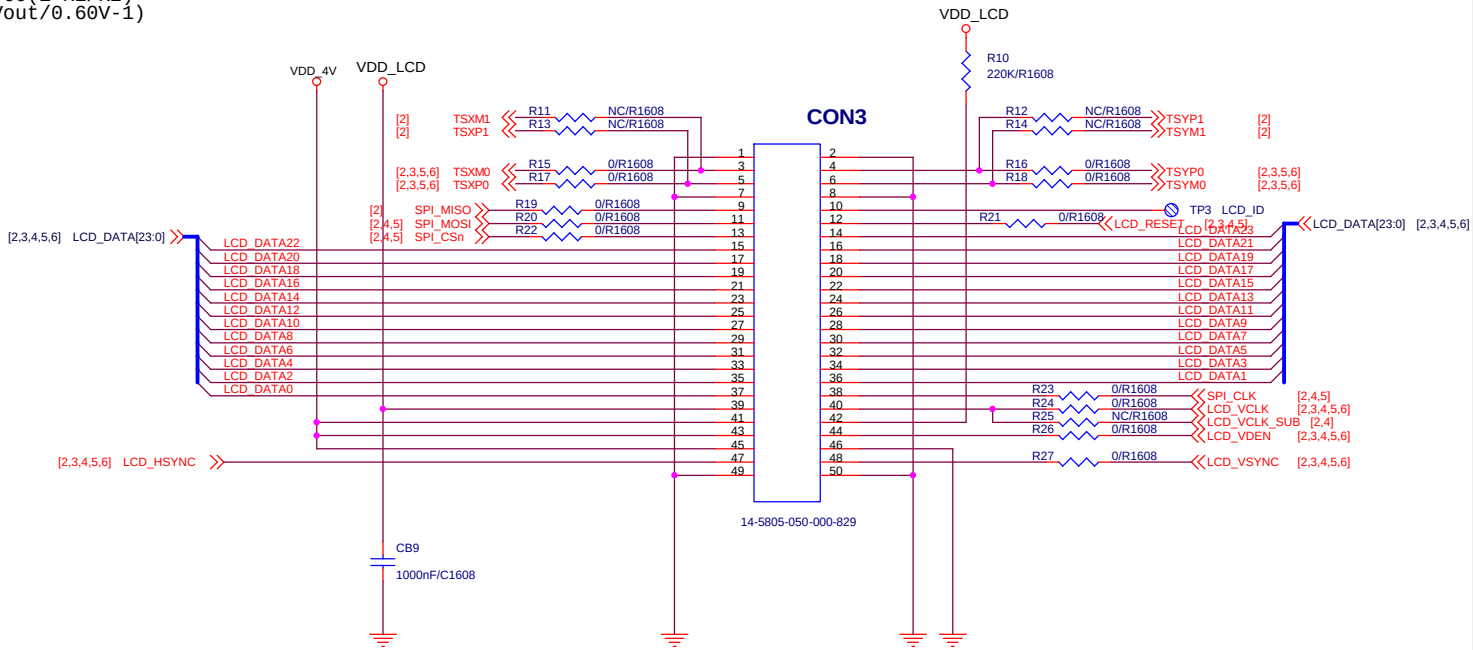
4.8inch WVGA(800x480)
LMS480KF02

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PC110 LCD Board (S5PC110 Evaluation Board)		
Size: A3	Document Number: 4.8inch WVGA(800x480)	Rev: 0.1
Date: Thursday, October 01, 2009	Sheet 3 of 4	

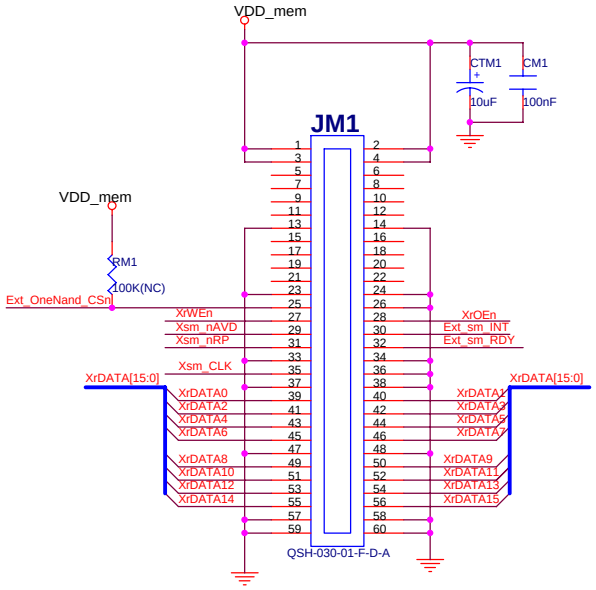


Vout=0.60(1+R1/R2)
R1=R2(Vout/0.60V-1)

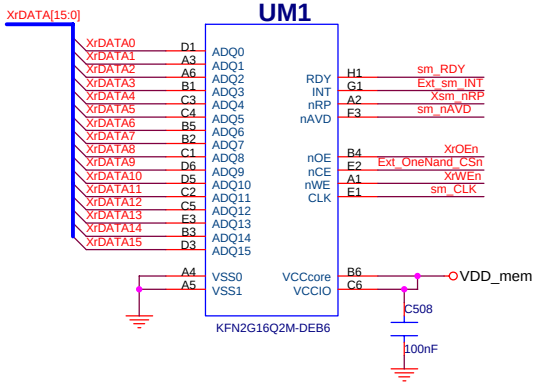




SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PC110 LCD Board (S5PC110 Evaluation Board)		
Size: A3	Document Number: Portrait WVGA(800x480)	Rev: 0.1
Date: Thursday, October 01, 2009	Sheet 4 of 4	



QTH/QSH Series (0.5mm)



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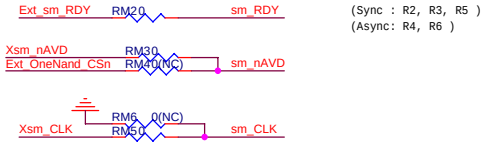
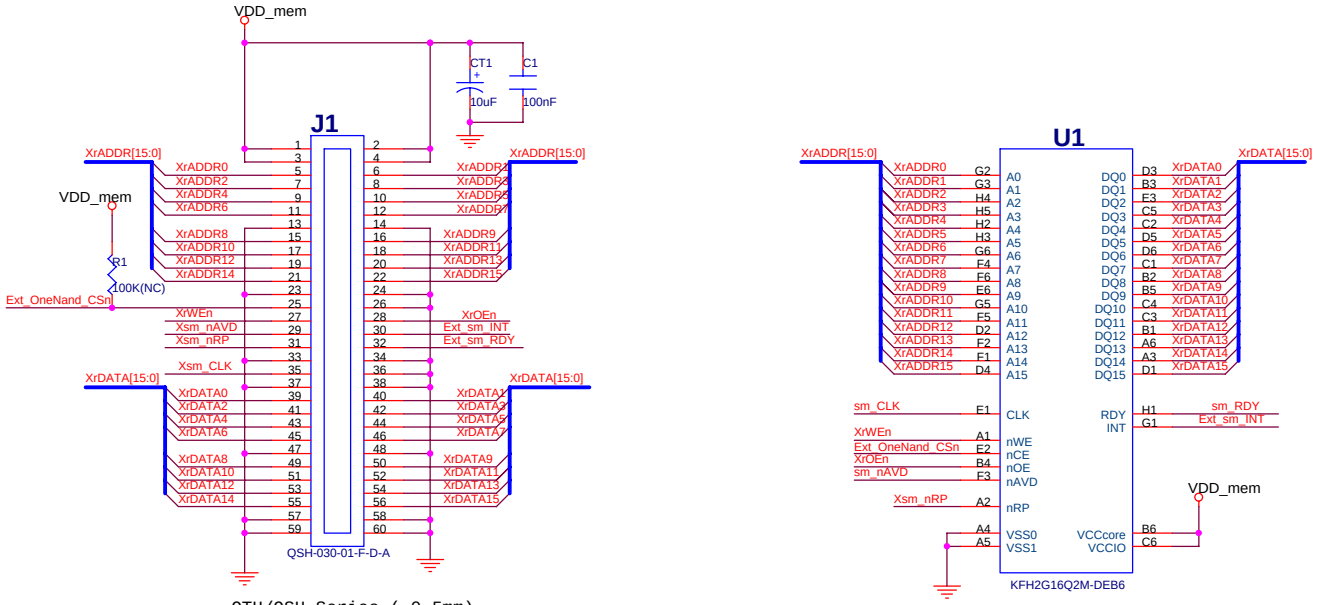
Mux OneNAND



(Sync : R2, R3, R5)
(Async: R4, R6)

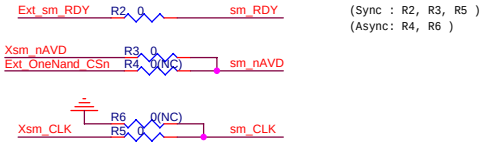
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2443 Evaluation Board		
Size: A3	Document Number: Ext. Mux OneNAND	Rev: Pre
Date: Wednesday, August 02, 2006	Sheet E2 of	



QTH/QSH Series (0.5mm)

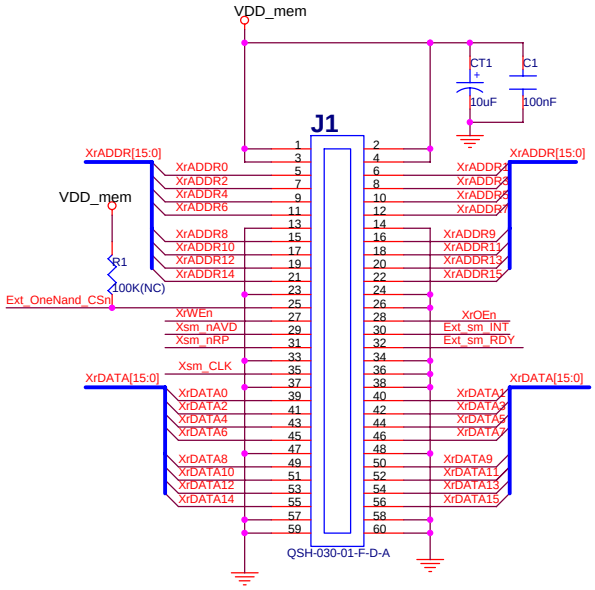
<Silk>

DeMux OneNAND

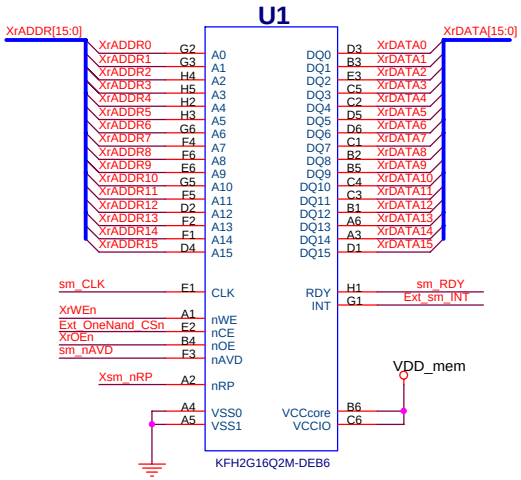


(Sync : R2, R3, R5)
(Async: R4, R6)

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2443 Evaluation Board		
Size: A3	Document Number: Ext. DeMux OneNAND	Rev: Pre
Date: Wednesday, August 02, 2006	Sheet E1 of	



QTH/QSH Series (0.5mm)



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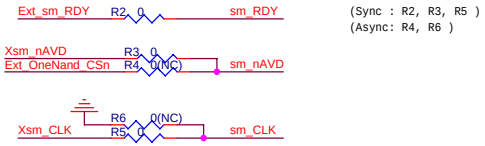
DeMux OneNAND



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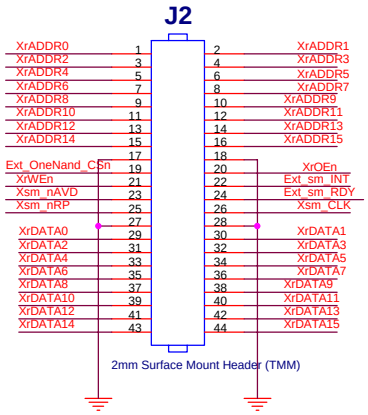
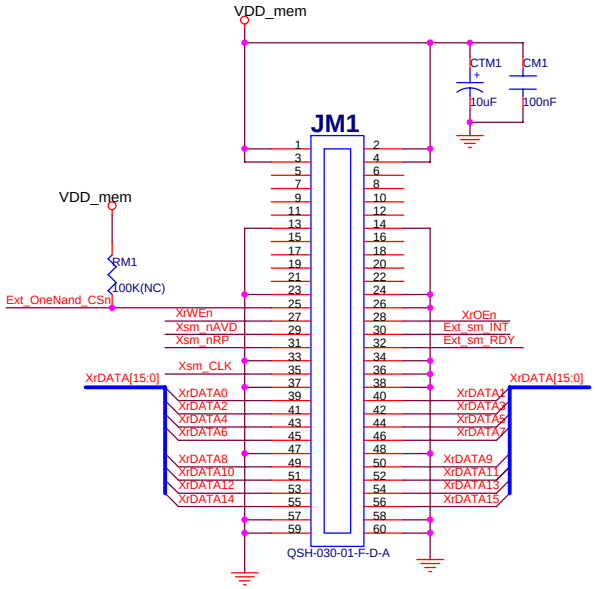
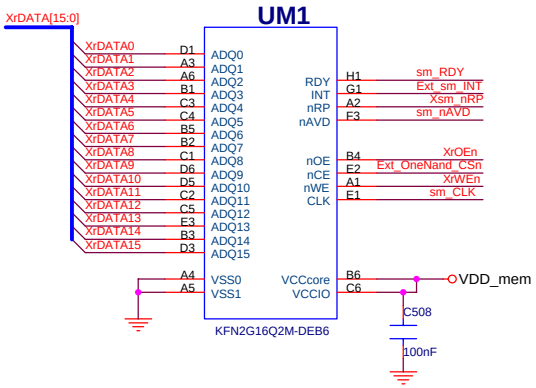
(Async: R4, R6)



SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2443 Evaluation Board		
Size: A3	Document Number: Ext. DeMux OneNAND	Rev: Pre
Date: Wednesday, August 02, 2006	Sheet E1 of	



QTH/QSH Series (0.5mm)



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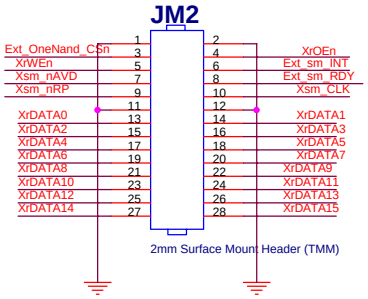
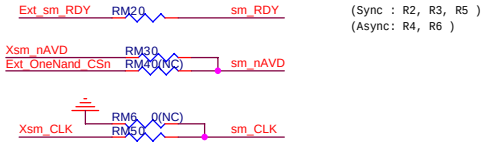
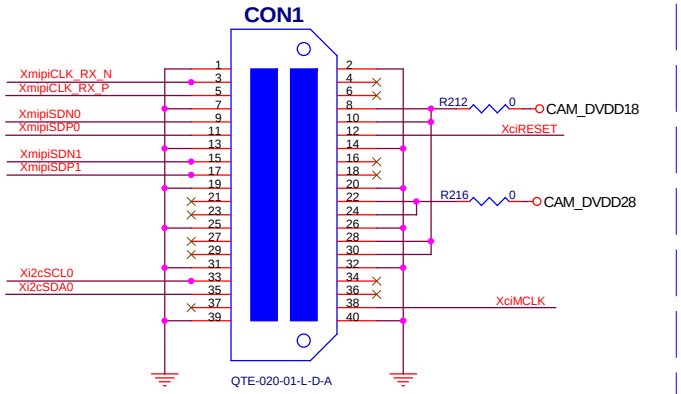
Mux OneNAND





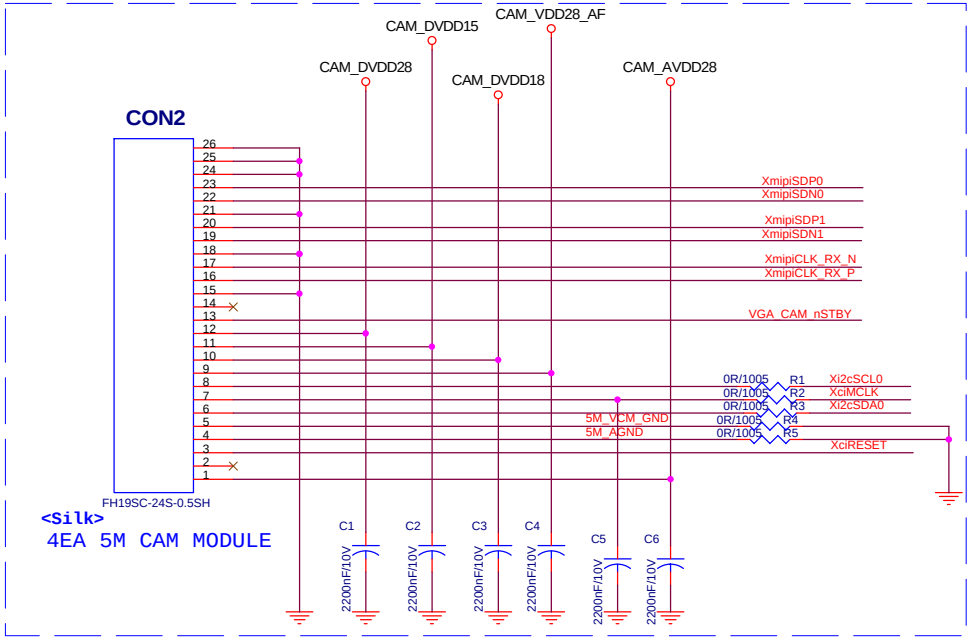
(Sync : R2, R3, R5)
(Async: R4, R6)

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2443 Evaluation Board		
Size: A3	Document Number: Ext. Mux OneNAND	Rev: Pre
Date: Wednesday, August 02, 2006	Sheet E2 of	



XmipiCLK_RX_N, XmipiCLK_RX_P, XmipiSDN0, XmipiSDP0, XmipiSDP1, XmipiSDN1
위 signal은 직선으로 연결 (500Mhz differential signal)

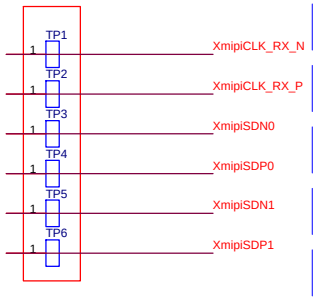
CON1



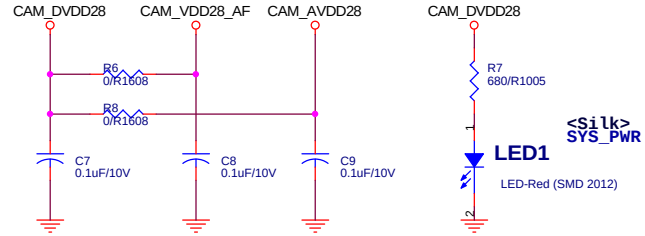
CON2

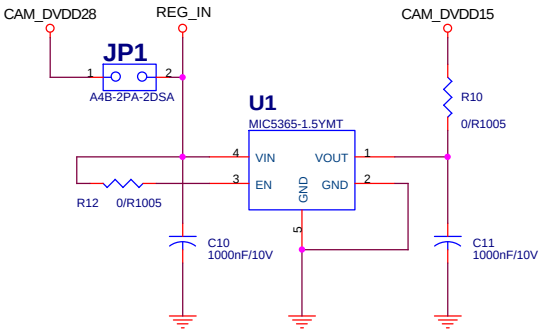
A

Be placed TPs on each lines.Not make stub.

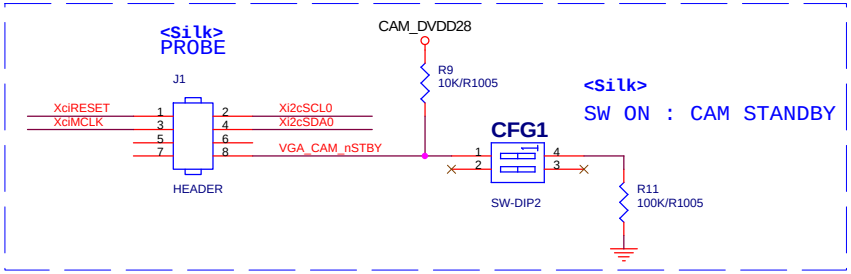


TP



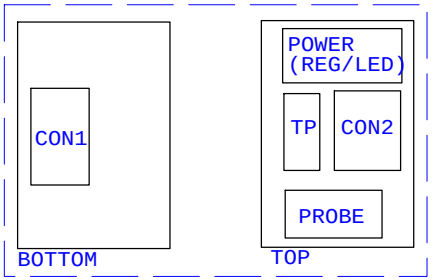


POWER



PROBE

A



Replacement Diagram

SAMSUNG ELECTRONICS CO.,LTD			
Title: SMDK_S5PC110_4EA Board (Daughter Board)			
Size: A3	Document Number		Rev: 0.0
Date: Thursday, May 21, 2009		Sheet 1 of 1	

MIPI-LCM&LAN Module B'd Schematics (for SMDK6440)

Revision	Date	Description
Rev 0.0	2009.03.06 (2009.02.17)	First Version

Table of Contents

Part Reference

<Component><Number>	
U	: Component or Regurator IC
C	: Capacitor
CB	: Capacitor Bypass
CT	: Capacitor Tantal
CTB	: Capacitor Tantal Bypass
CP	: Capacitor return Path on power plane
J	: Jumper
JB	: CPU or Base connector
JP	: Jumper Power
R	: Resistor
RA	: Resistor Array
RP	: Resistor Power
VR	: Variable Resistor
L	: Inductor
FB	: Ferrite Bead
OSC	: Oscillator
X	: X-tal (Crystal)
Q	: Transistor or FET
D	: Diode
ZD	: Zener Diode
LED	: LED Diode
SW	: SWitch Tact/Push
CON	: CONnector
CFG	: ConFiGure switch (DIP/Slide)

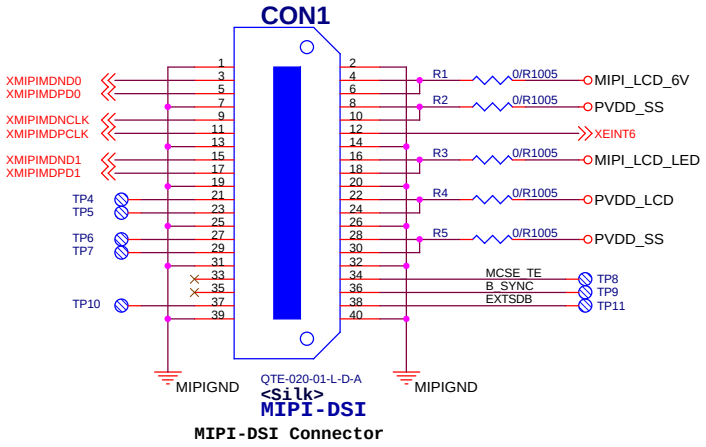
<Component><Number>	
TP	: Test Point (SMD)
TPH	: Test Point Hole (Through Hole)
MTH	: Mount Through Hole
MOD	: MODule Interface connector

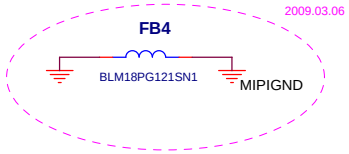
SAMSUNG ELECTRONICS CO., LTD

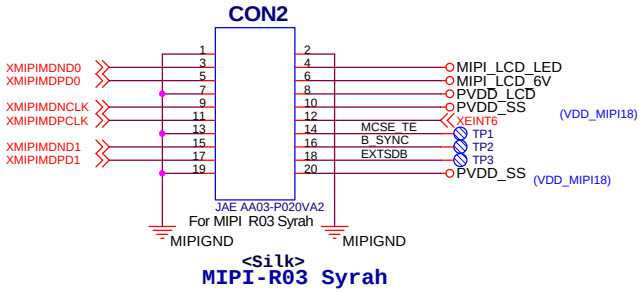
Title: MIPI-LCM&LAN Module B'd (for SMDK6440)

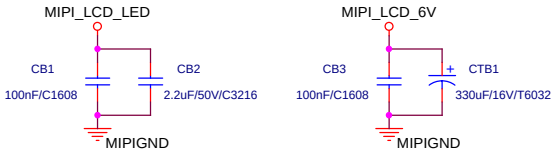
Size: A3 | Document Number: Revision History | Rev: 0.0

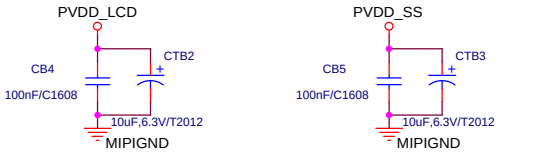
Date: Friday, March 06, 2009 | Sheet 1 of 3

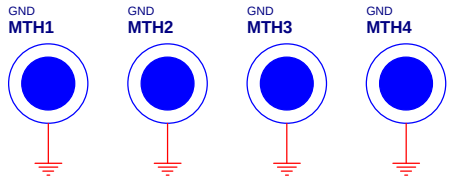




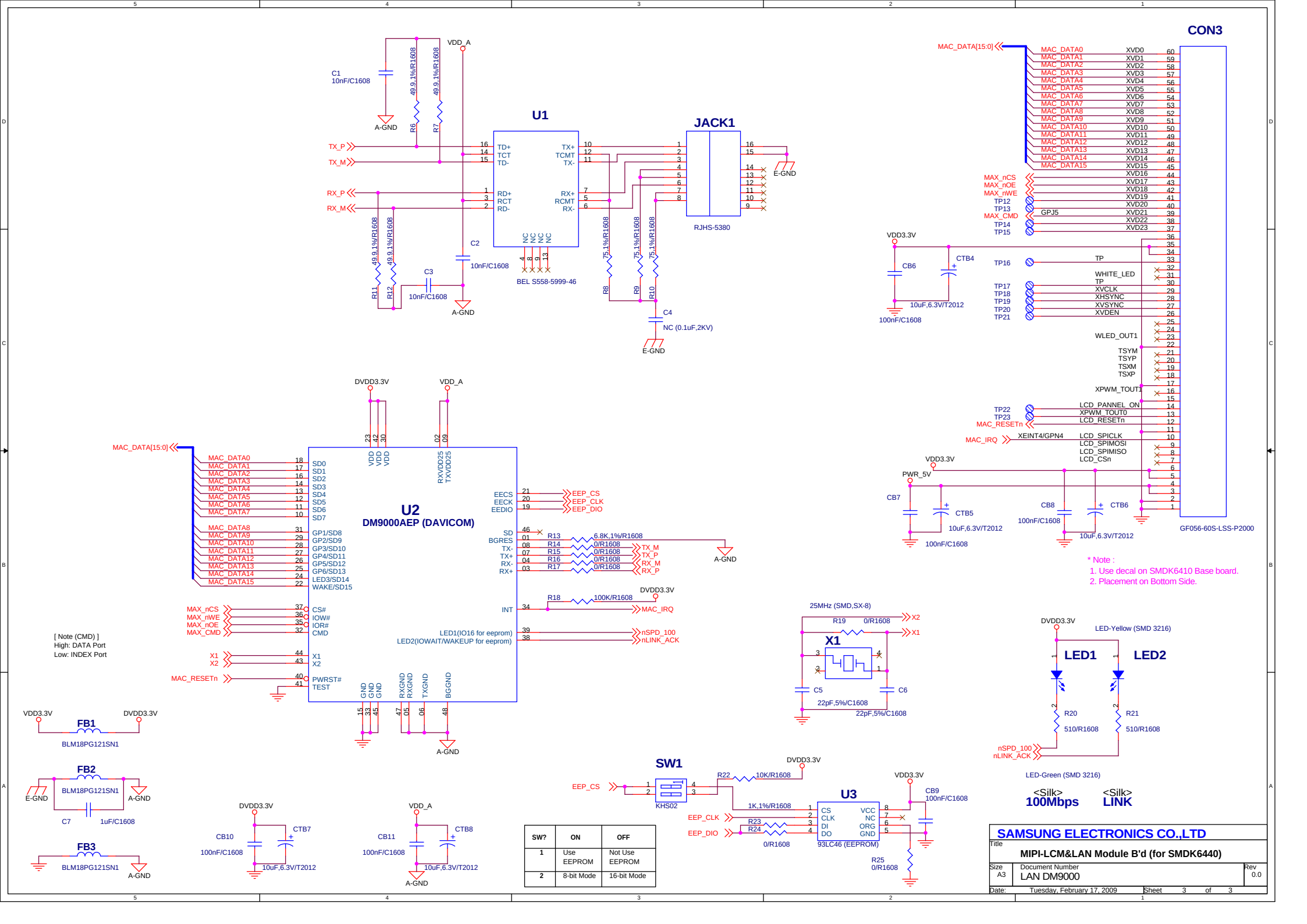








SAMSUNG ELECTRONICS CO.,LTD		
Title: MIPI-LCM&LAN Module B'd (for SMDK6440)		
Size: A3	Document Number: MIPI-LCM	Rev: 0.0
Date: Friday, March 06, 2009	Sheet 2 of 3	



SW?	ON	OFF
1	Use EEPROM	Not Use EEPROM
2	8-bit Mode	16-bit Mode

Size	Document Number	Rev
A3	LAN DM9000	0.0

Date: Tuesday, February 17, 2009 Sheet 3 of 3